Authenticache: Harnessing Cache ECC for System Authentication

Anys Bacha and Radu Teodorescu

Department of Computer Science and Engineering

The Ohio State University

http://arch.cse.ohio-state.edu

THE OHIO STATE UNIVERSITY

COMPUTER ARCHITECTURE RESEARCH LAB

Security and Everyday Computing

Security is now crucial to all computing markets, especially with the advent of IoT

Security Challenges

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- Password management
  - Complexity due to different accounts having policies

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- Secure key storage
  - Increases complexity for low cost IoT devices

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- Software as a Service
  - Personal device at workplace increasing security risks

Physical Unclonable Functions (PUF)

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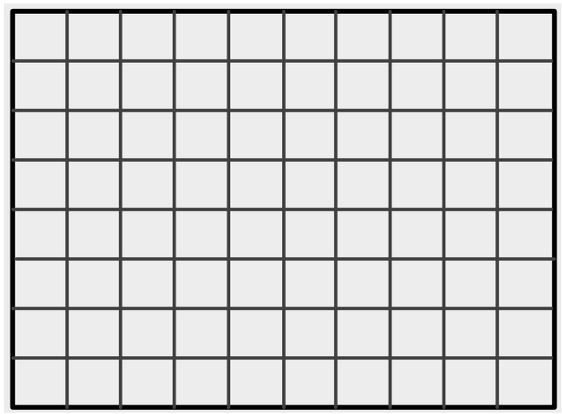
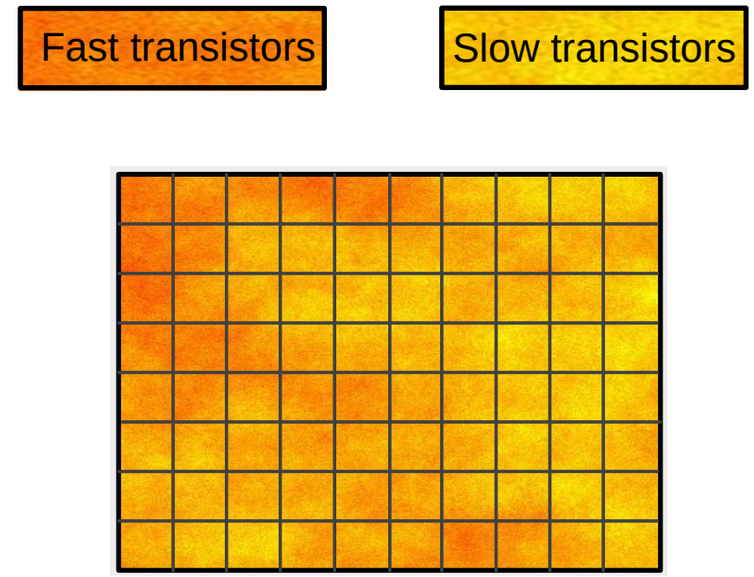


Chip

Physical Unclonable Functions (PUF)



Chip

- Exploit randomness in silicon

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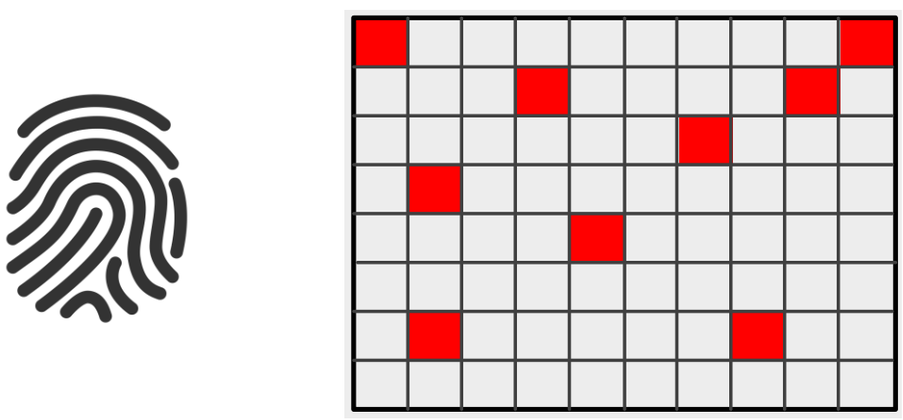

Chip

Silicon Fingerprints

- Exploit randomness in silicon
- Systematic outputs unique to device

PUF System Authentication

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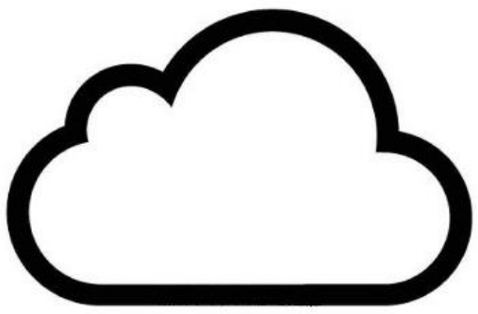
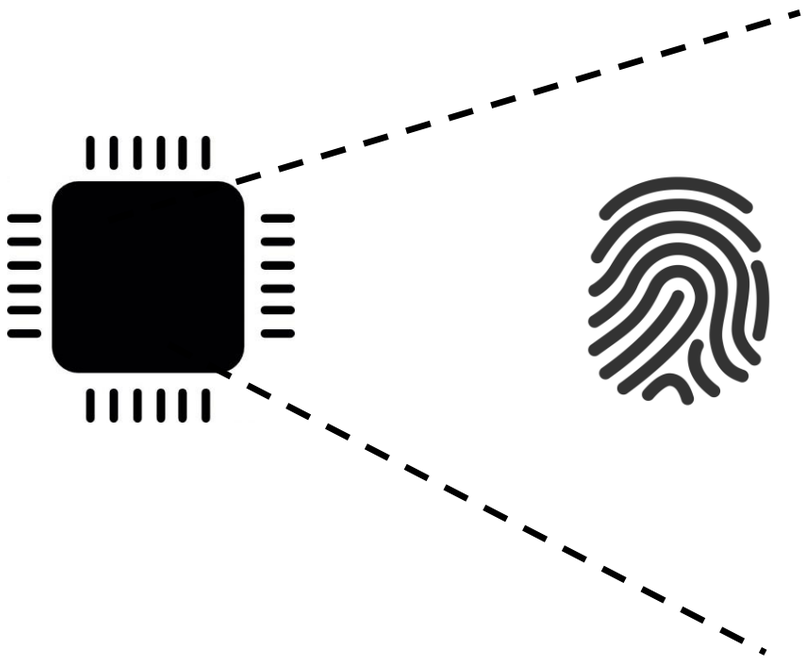
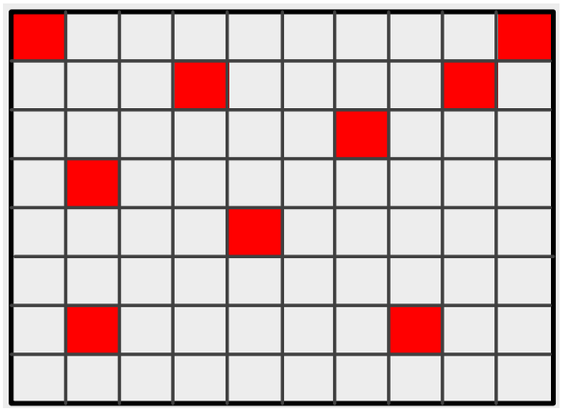
Enrollment







Silicon Fingerprints

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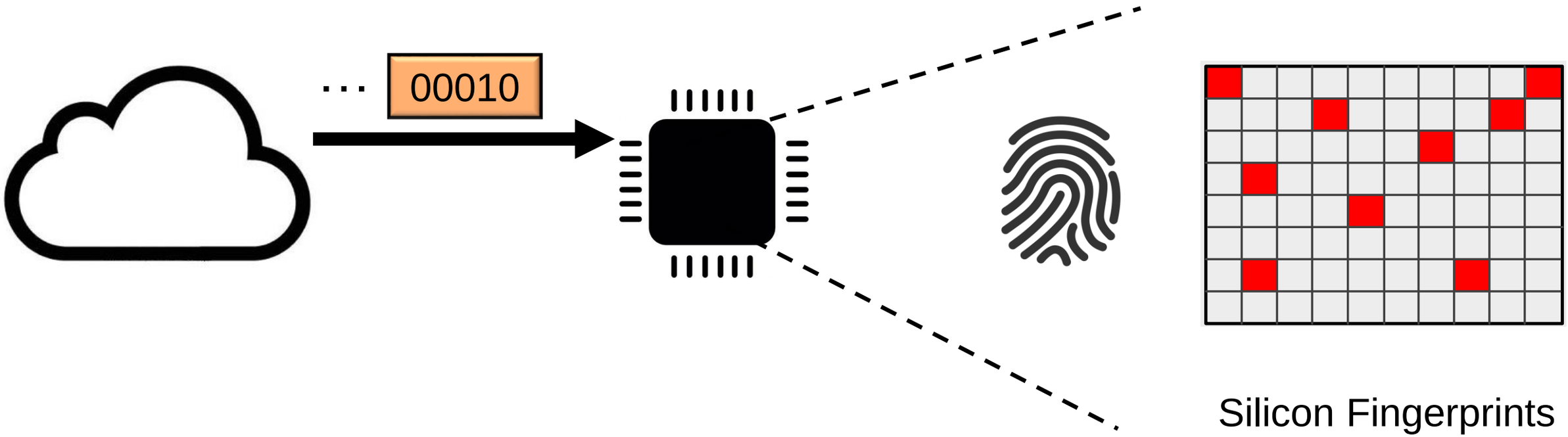

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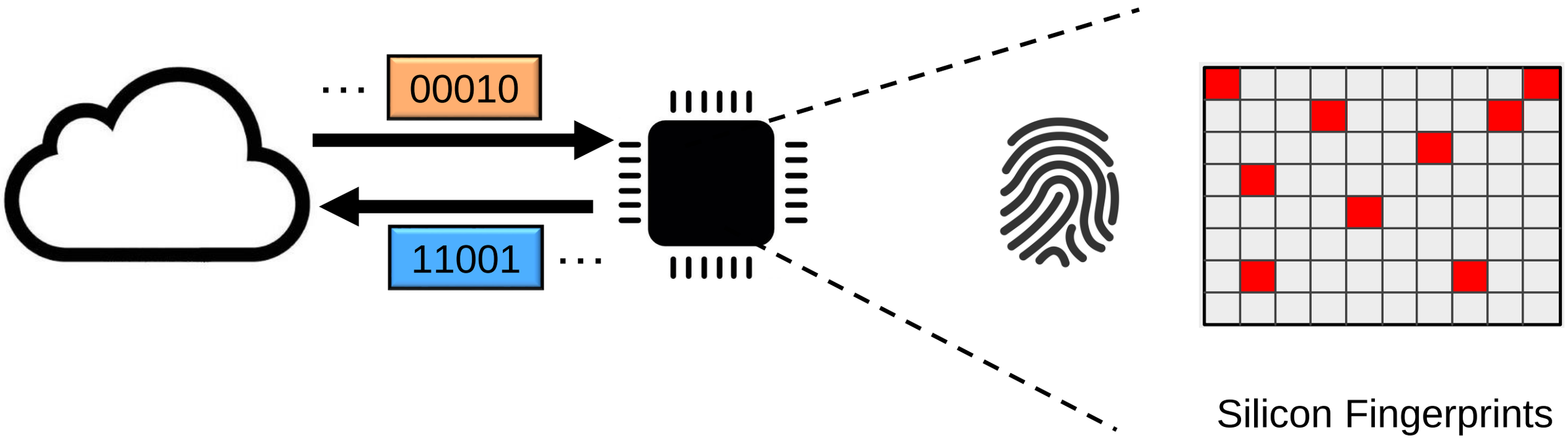

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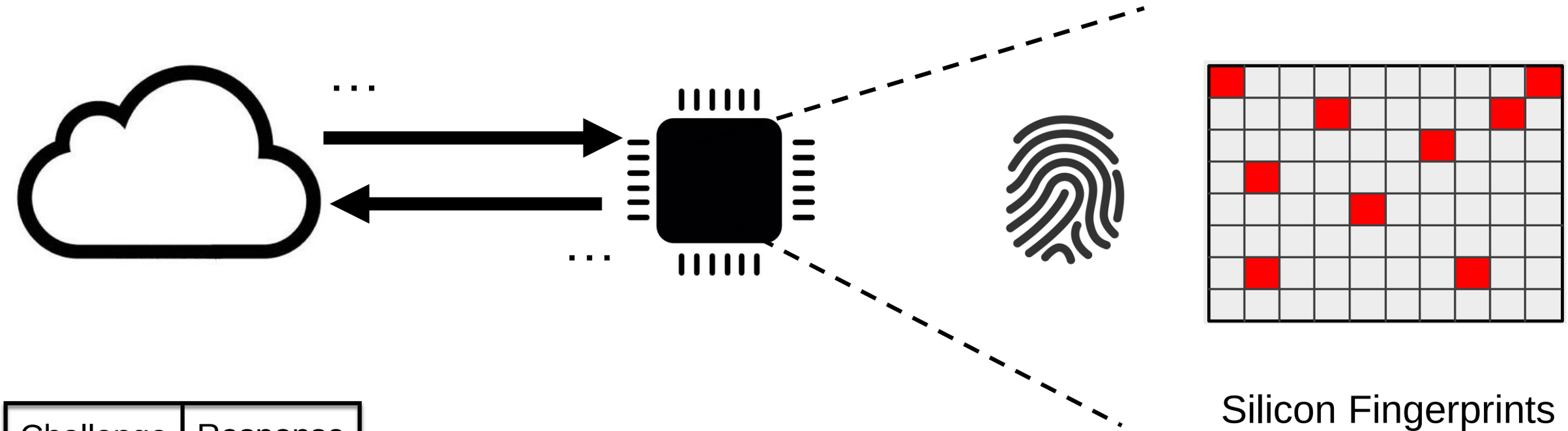

Challenge	Response
01100	00110
…	…
00010	11001

Silicon Fingerprints

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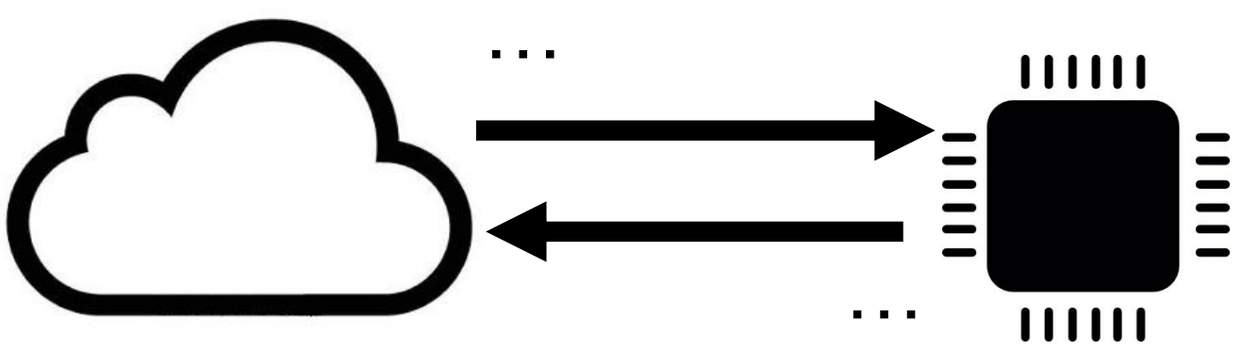

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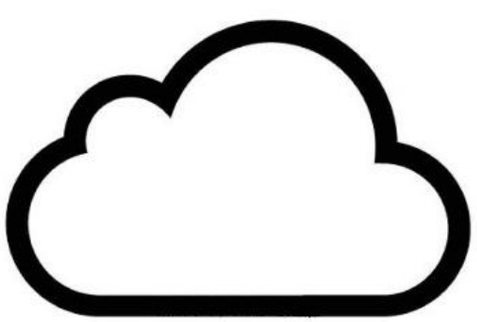

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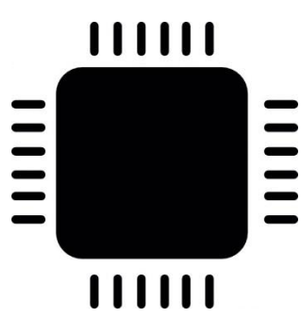

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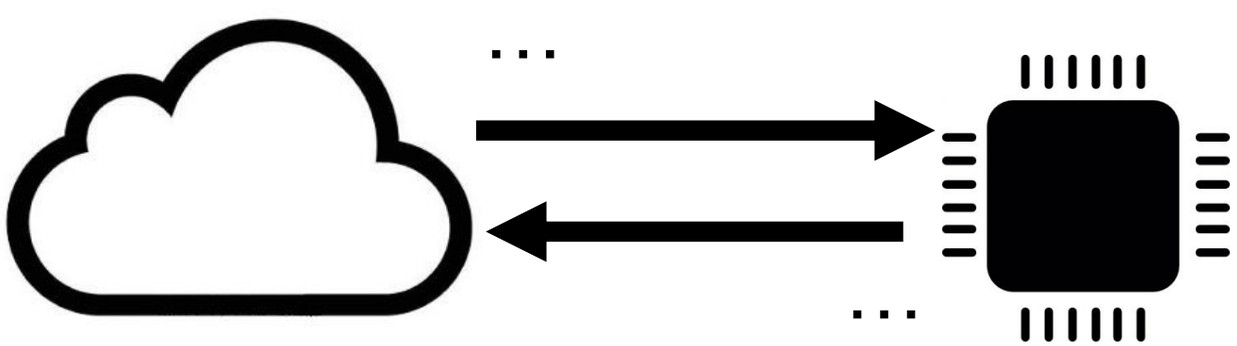

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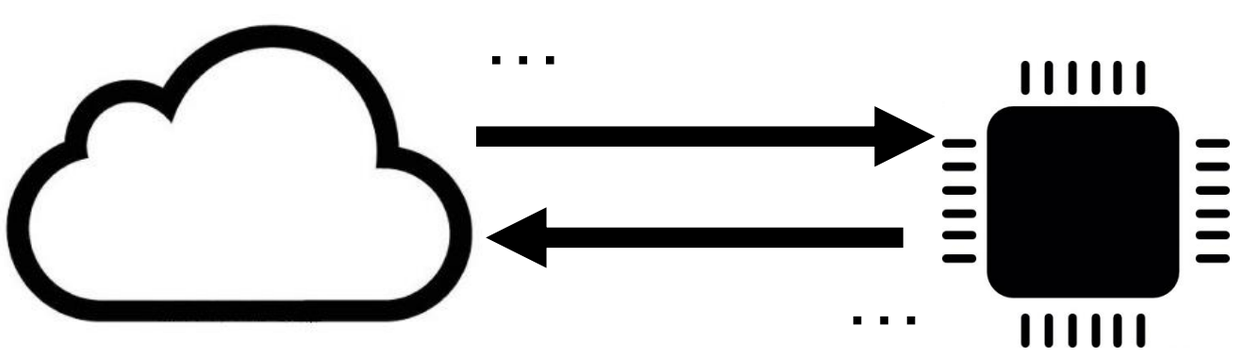

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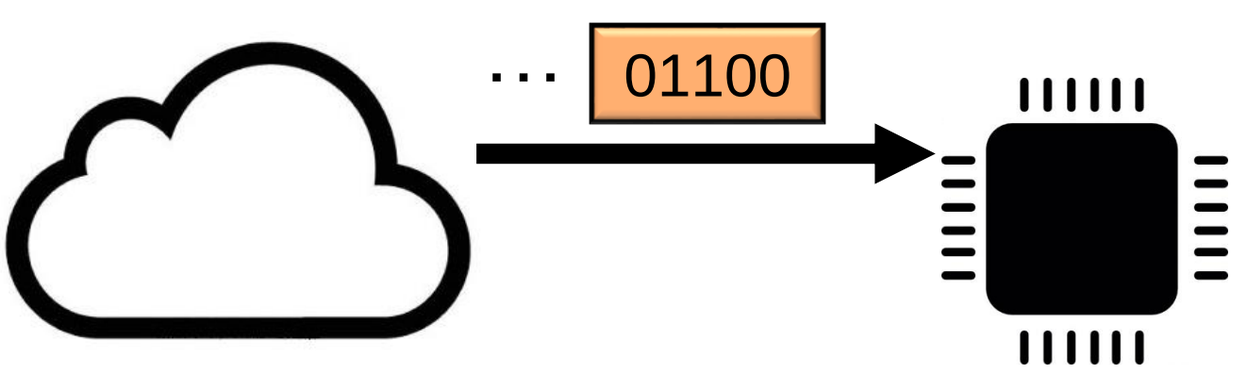

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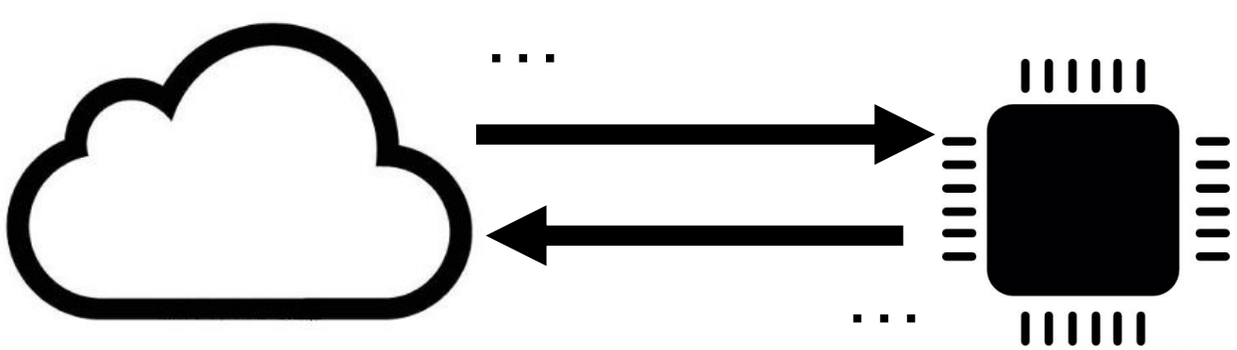

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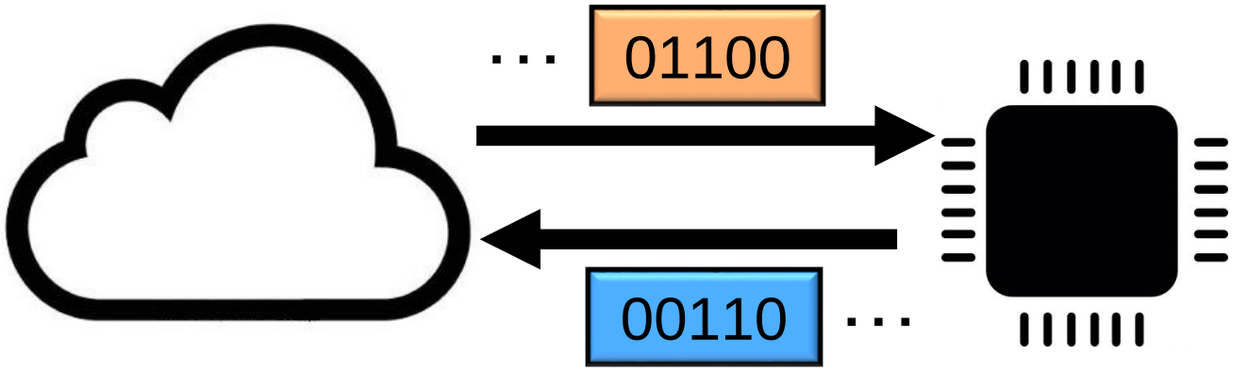

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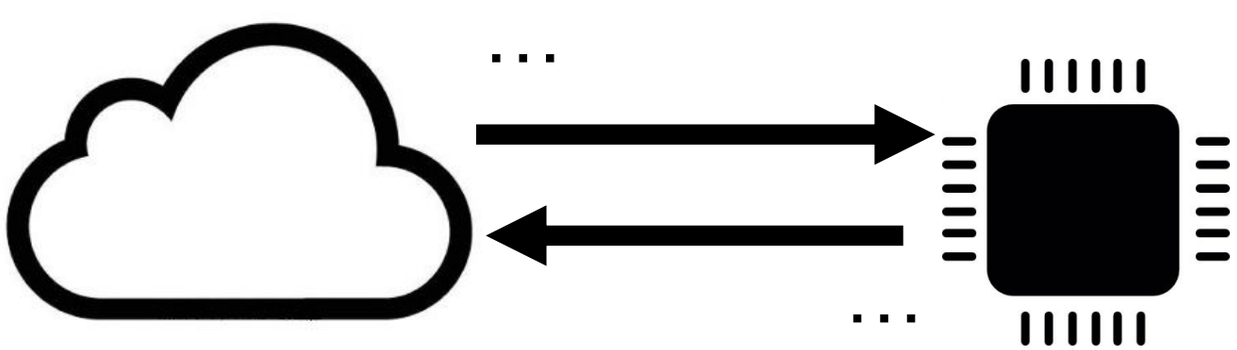

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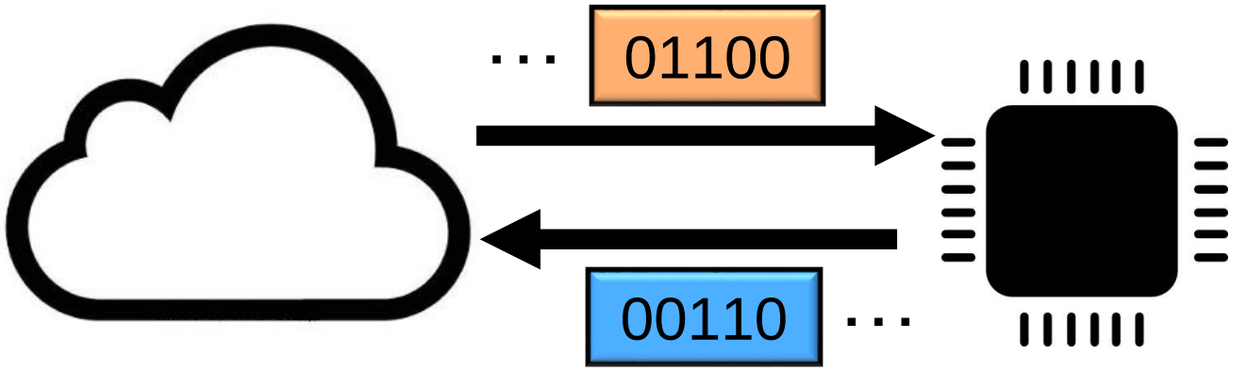

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Related Work

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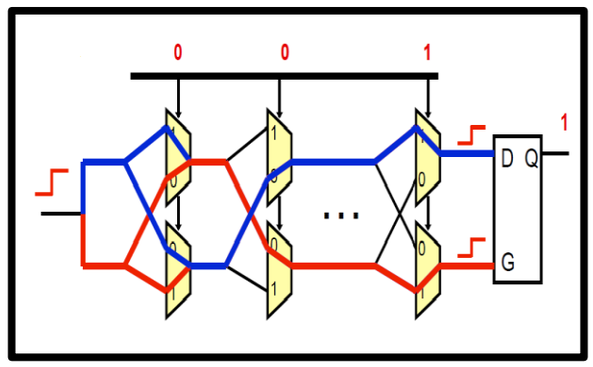
  - Signal traversing maze of cascaded switch blocks



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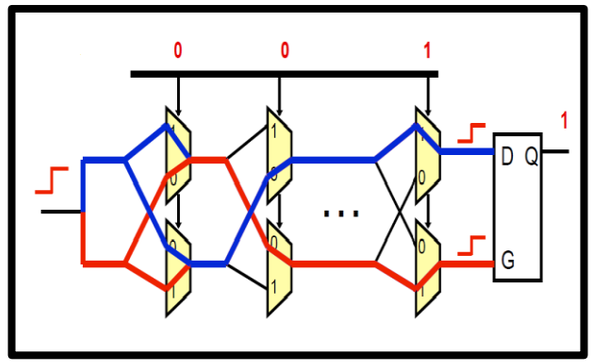
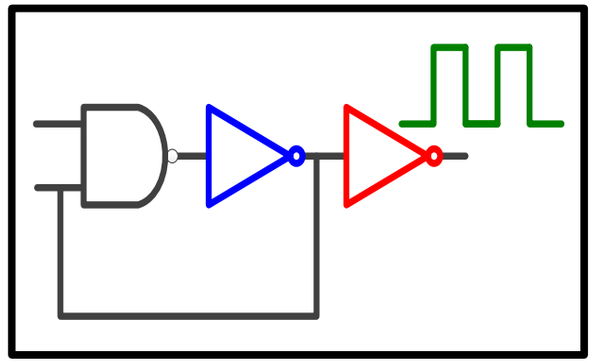


Aribiter PUF

- Ring Oscillator PUF (Suh et al. DAC'07)
  - Delay loops feeding oscillations into counters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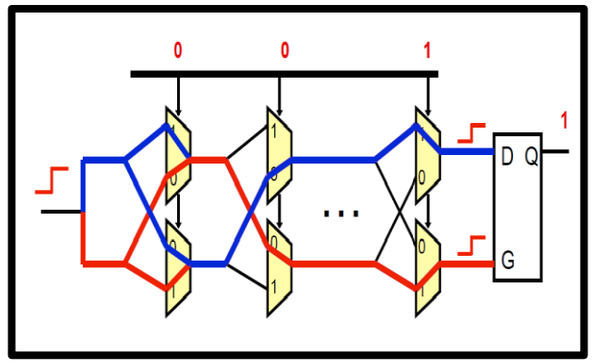

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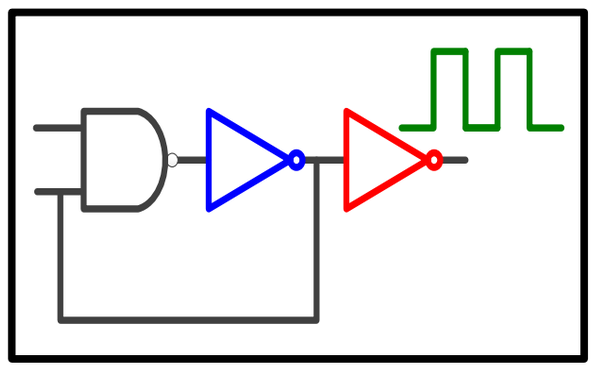
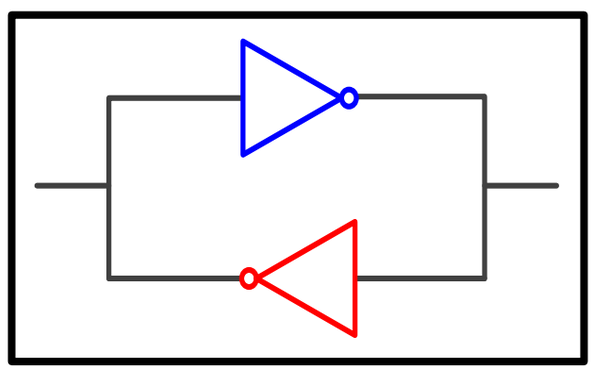

Ring Oscillator PUF

- SRAM PUF (Guajardo et al. CHES'07)
  - Power-on states of 6T SRAM cell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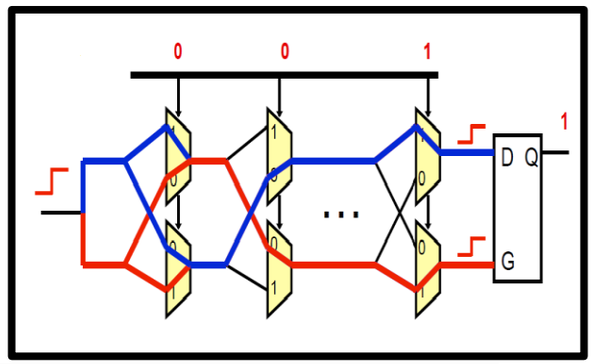

Authenticache: No custom hardware

On-chip error correction logic in processor caches

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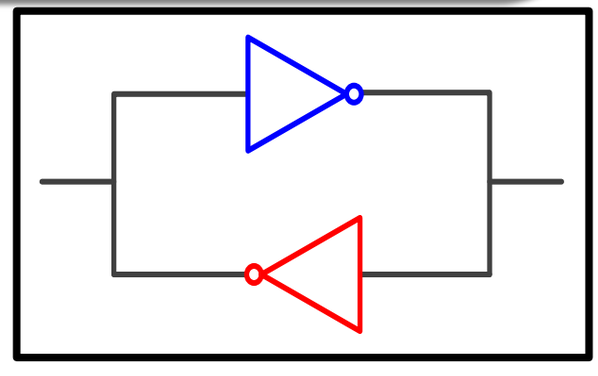

SRAM PUF

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Intel 9560 Processor

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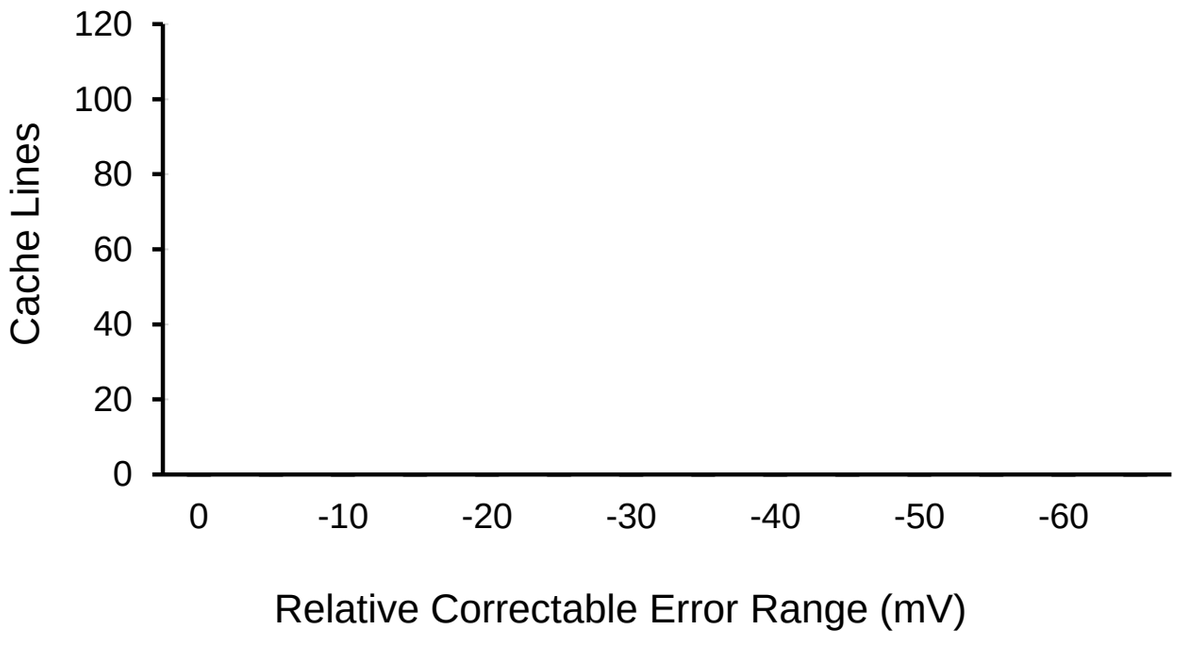

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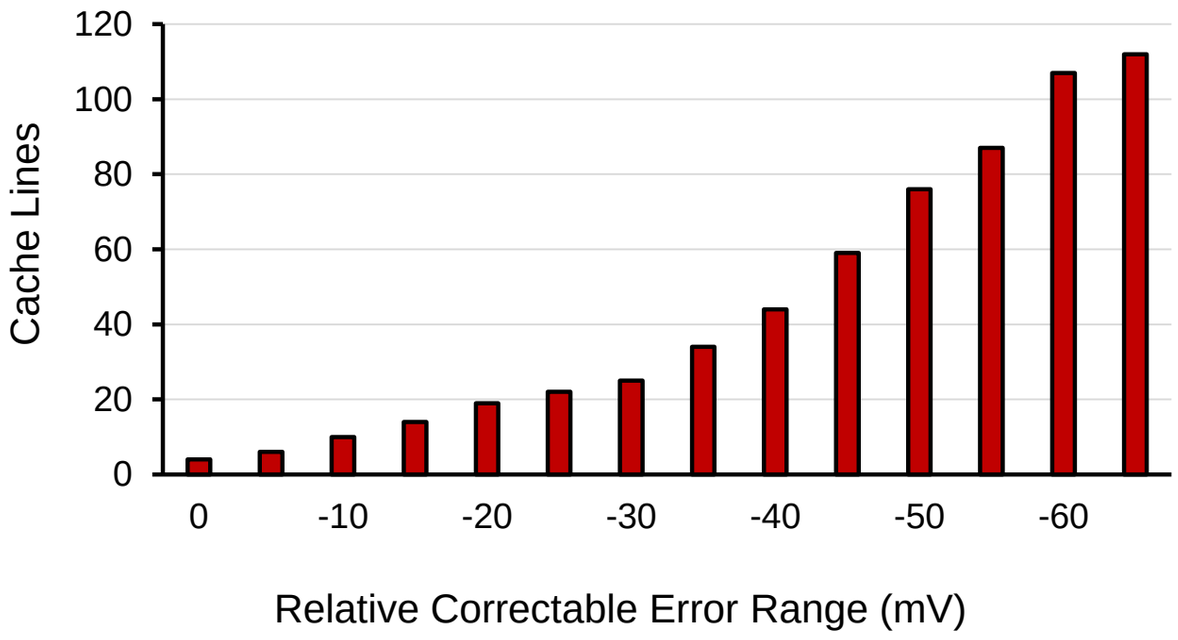

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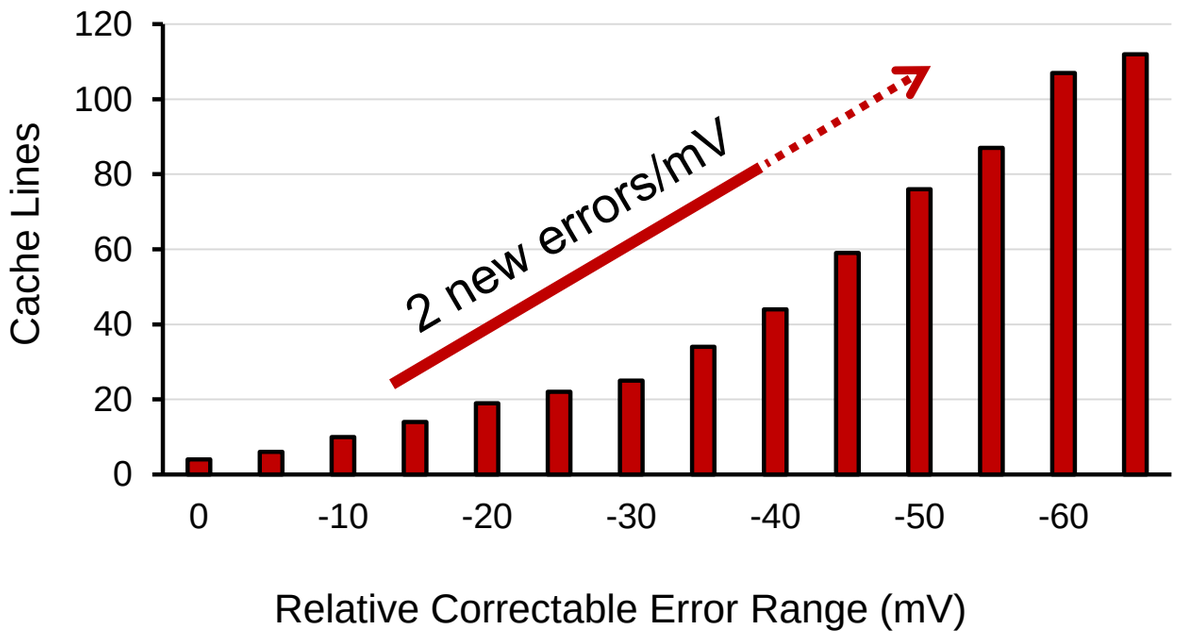

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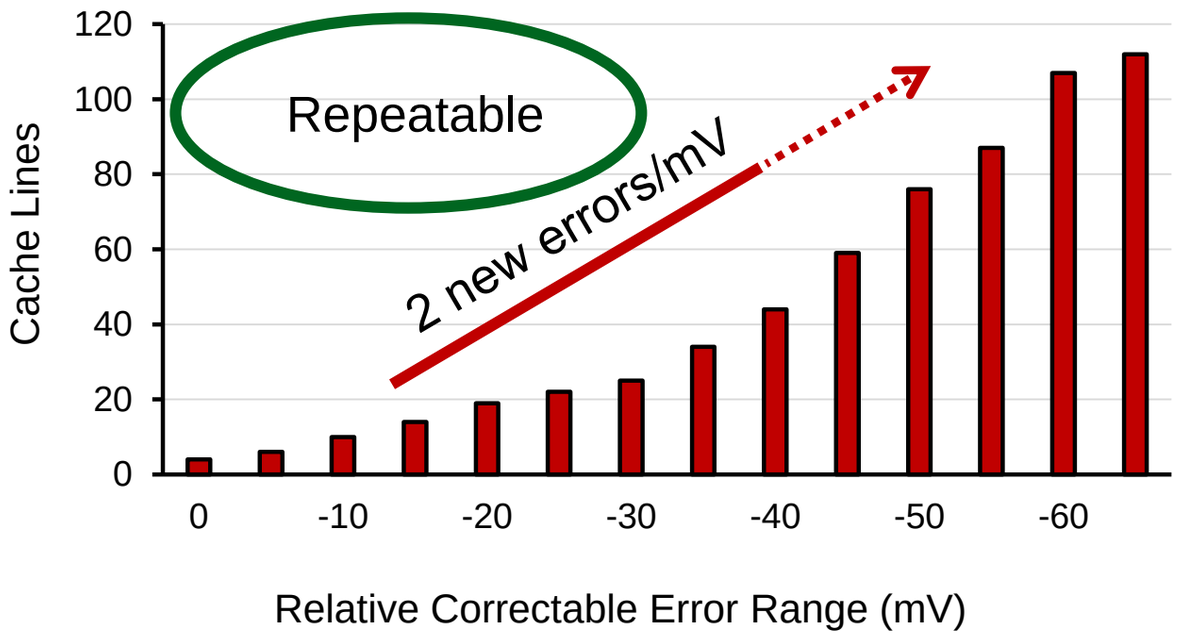

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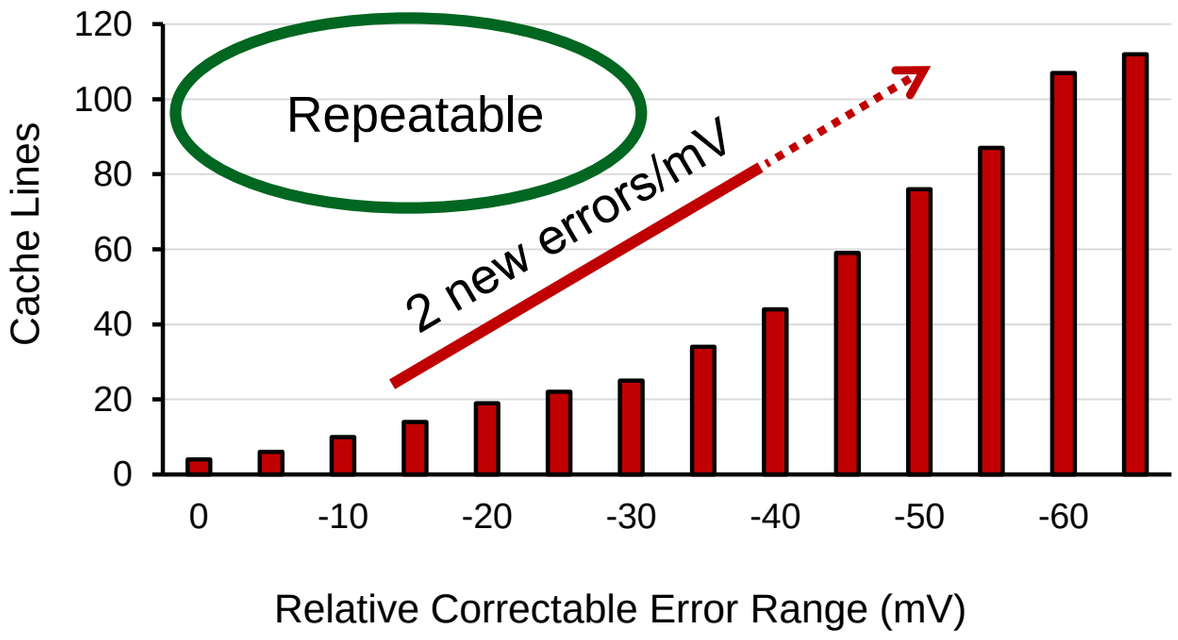

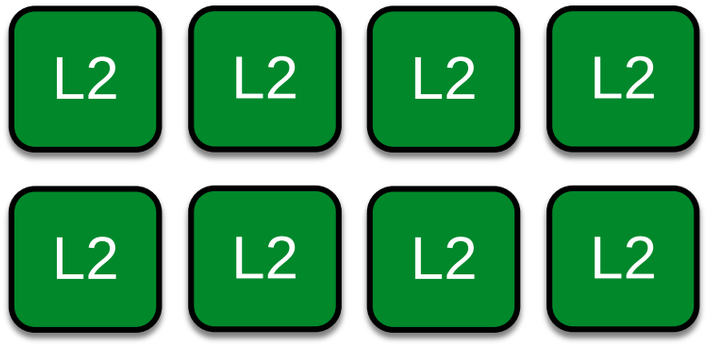

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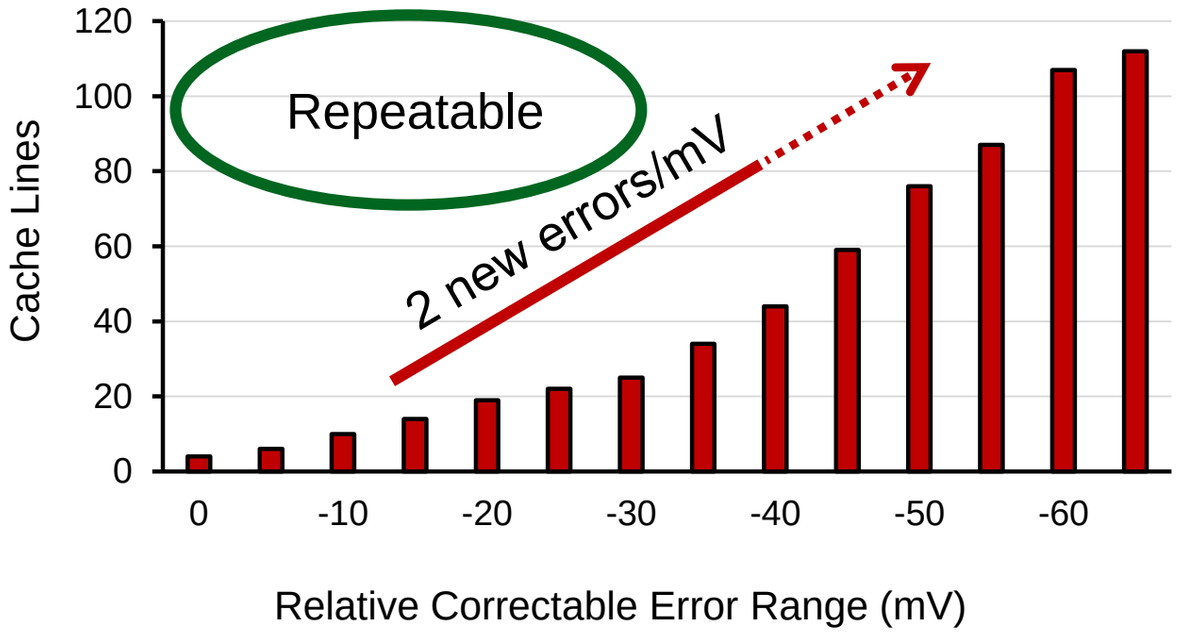

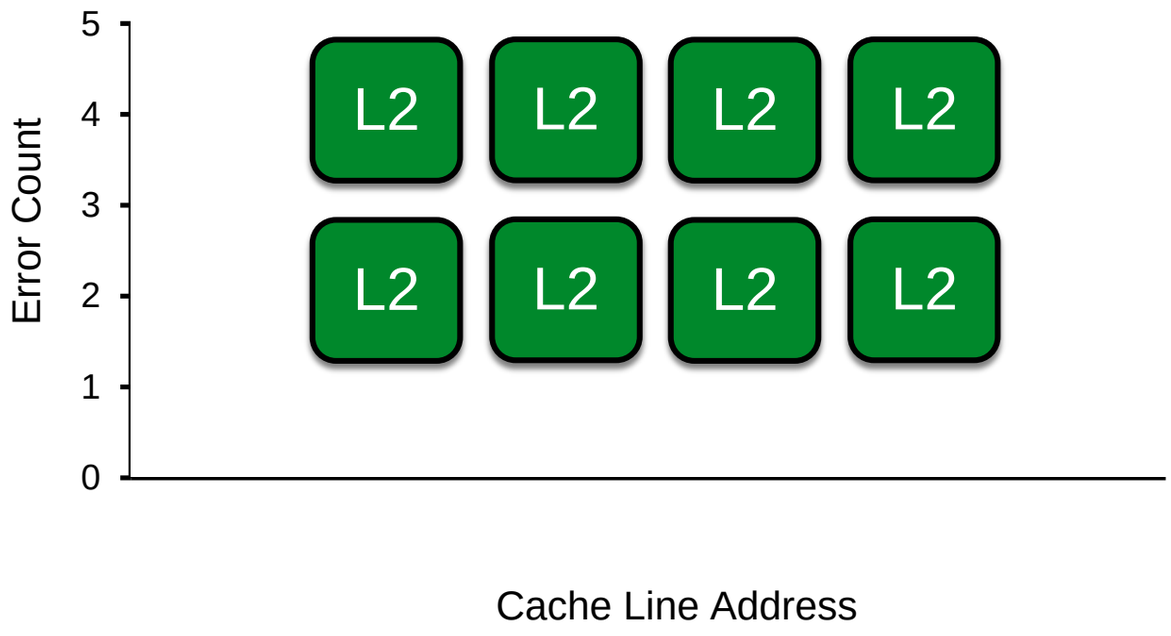

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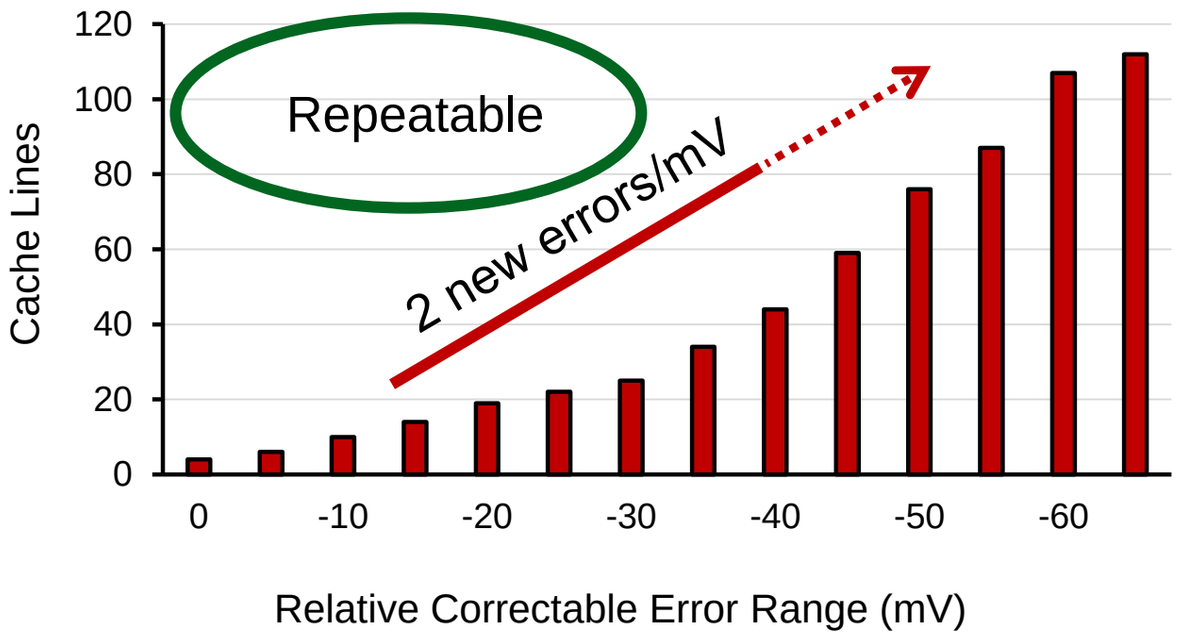

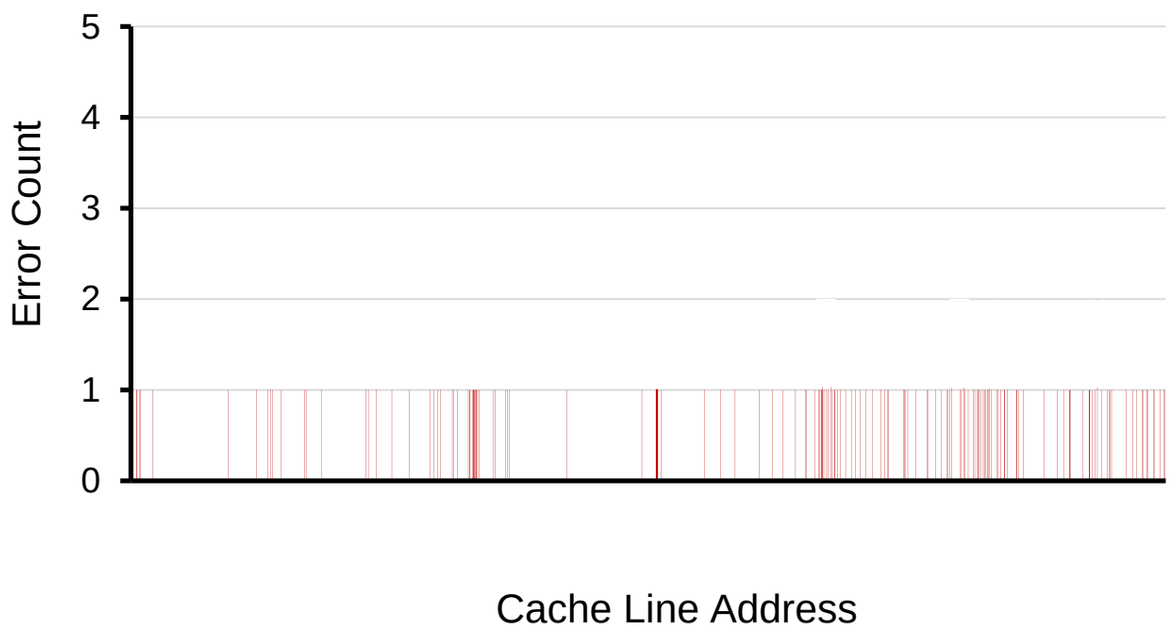

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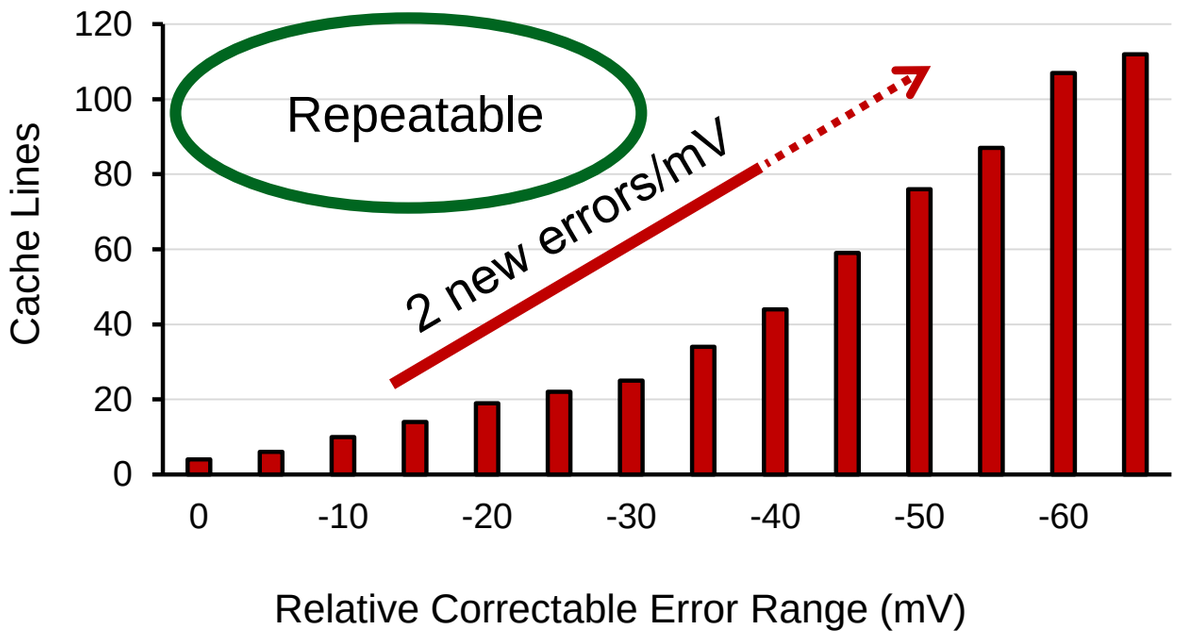

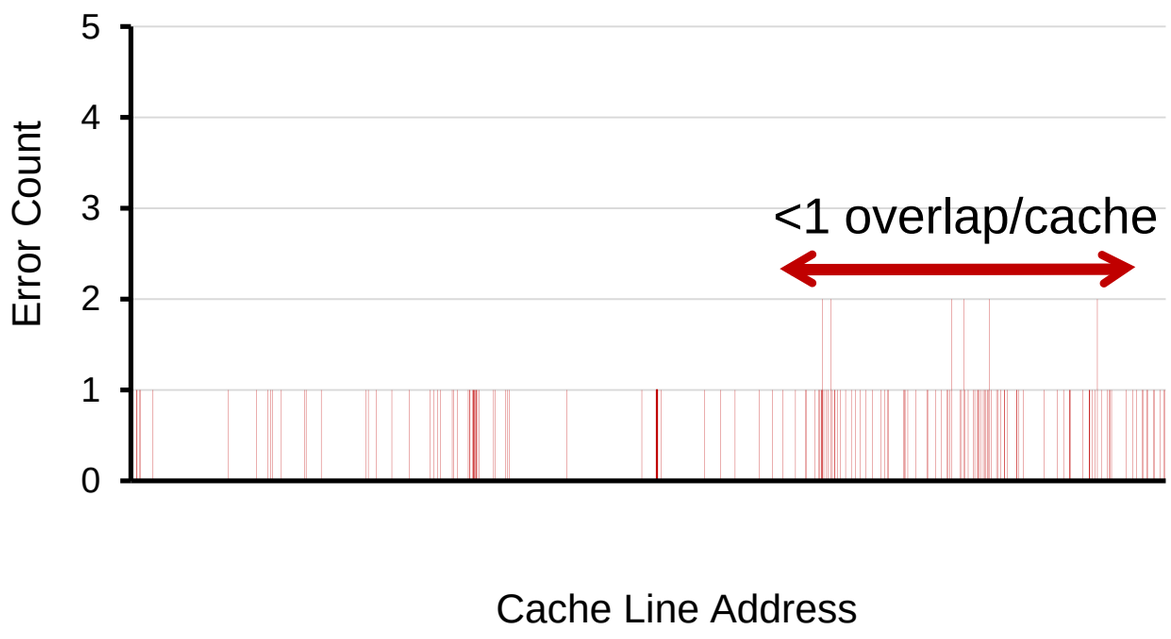

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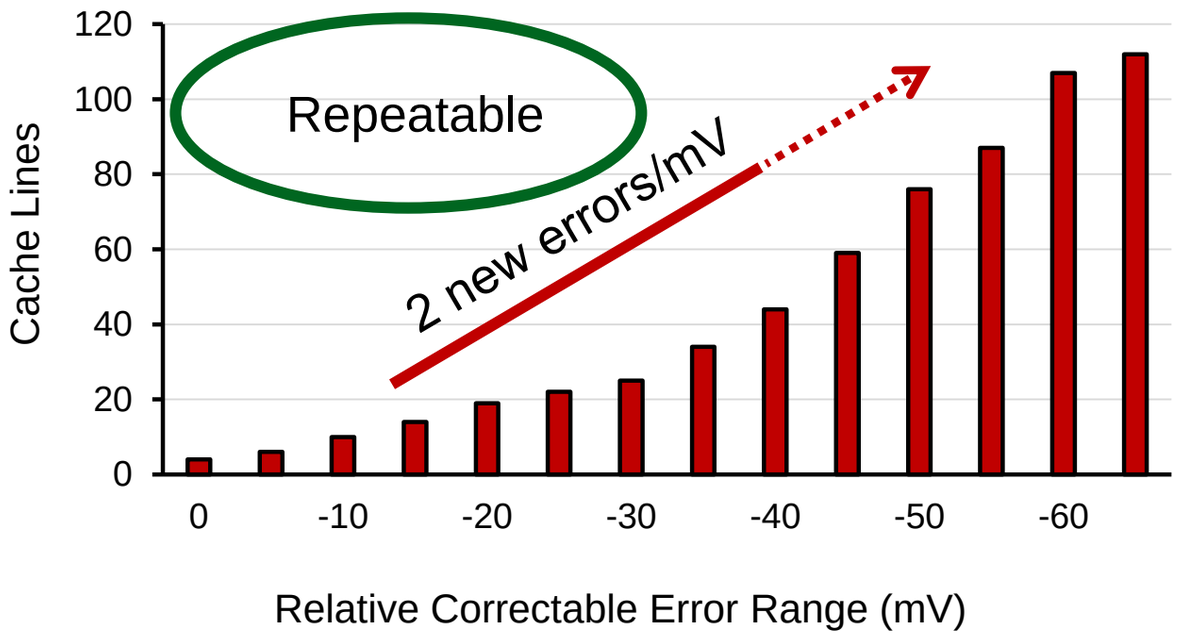

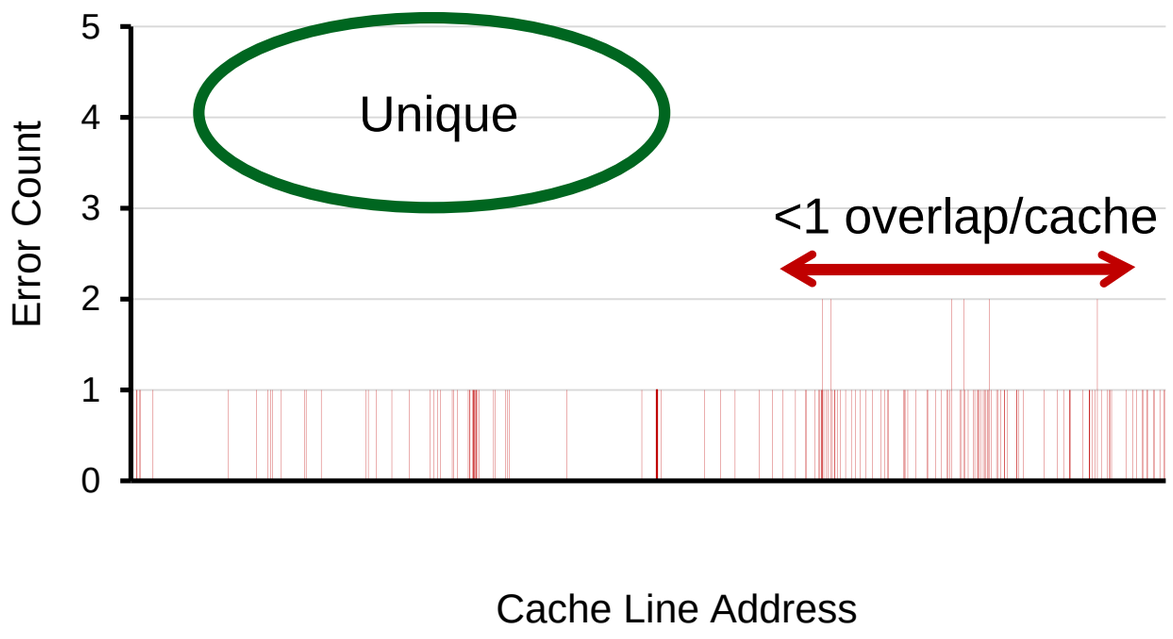

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The Authenticache System

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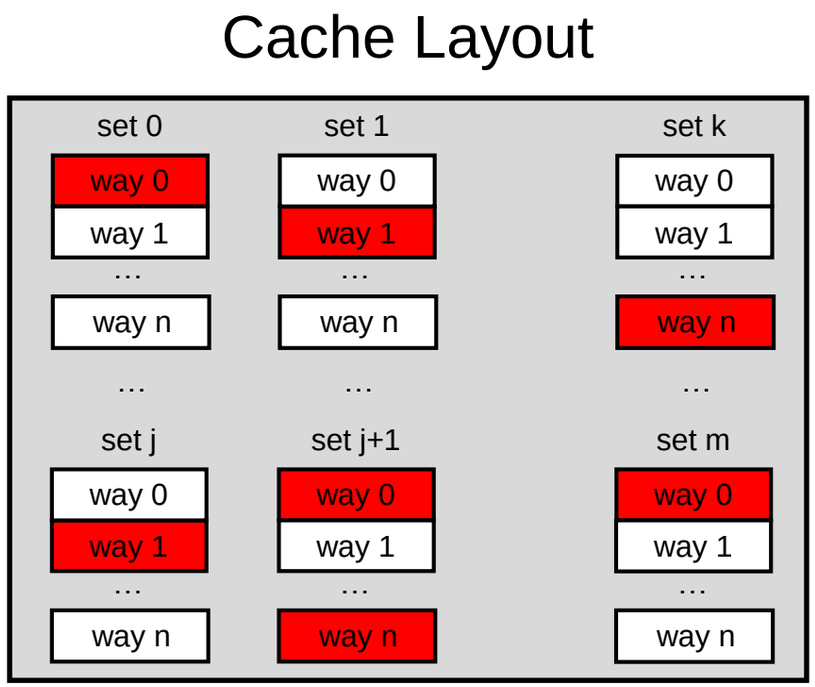

- Exploit process variation in LLC for randomness

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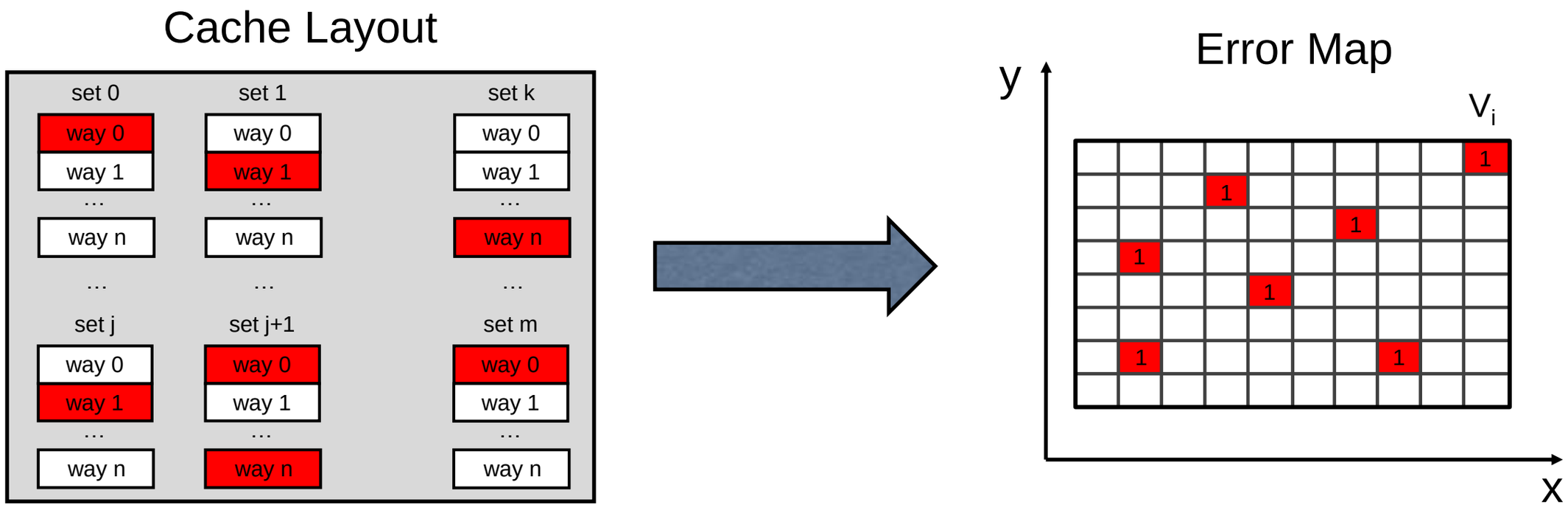

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- Construct cache maps as a function of voltage and correctable errors

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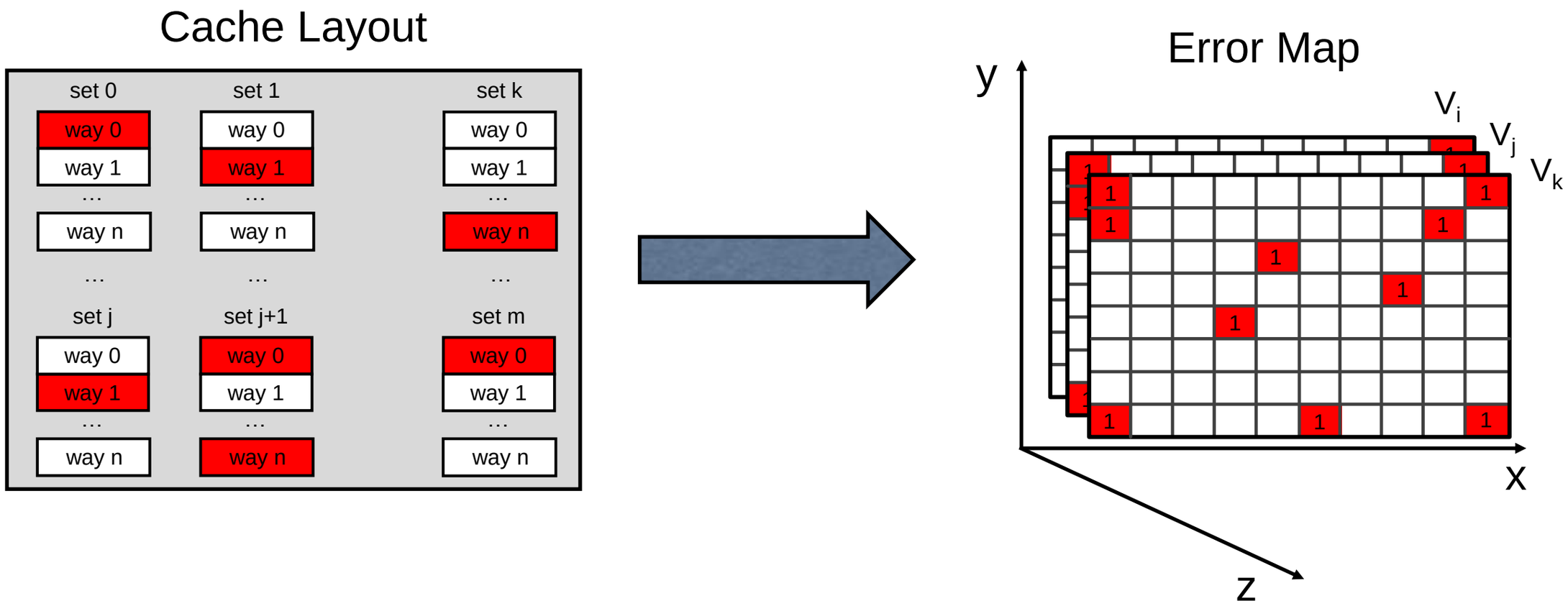

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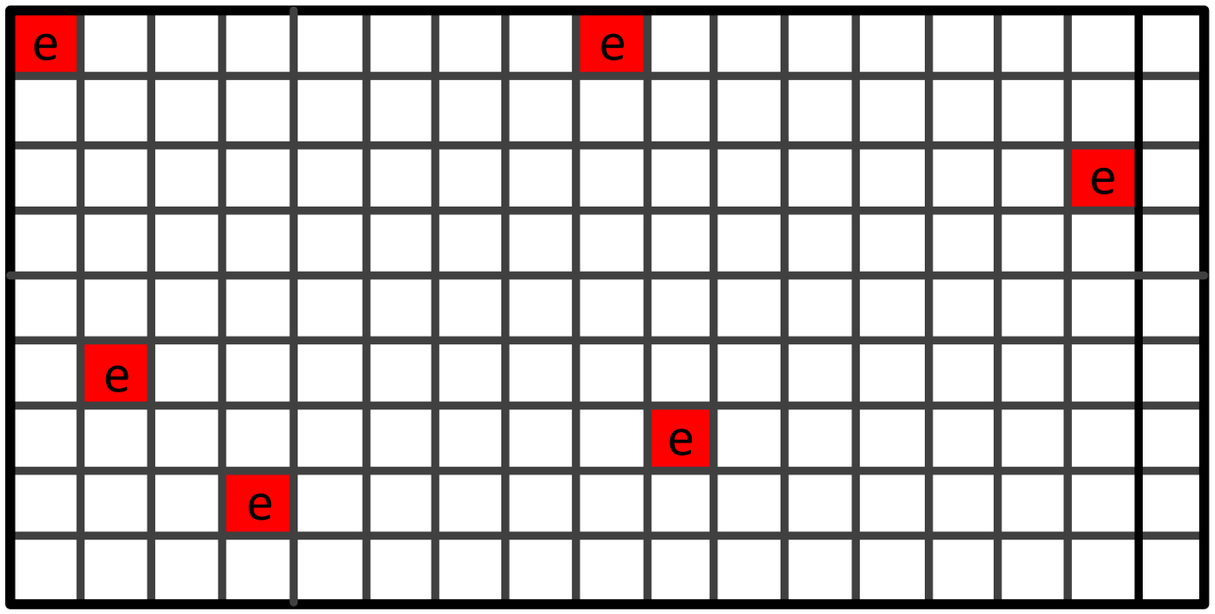
Challenge and Response

Error Map



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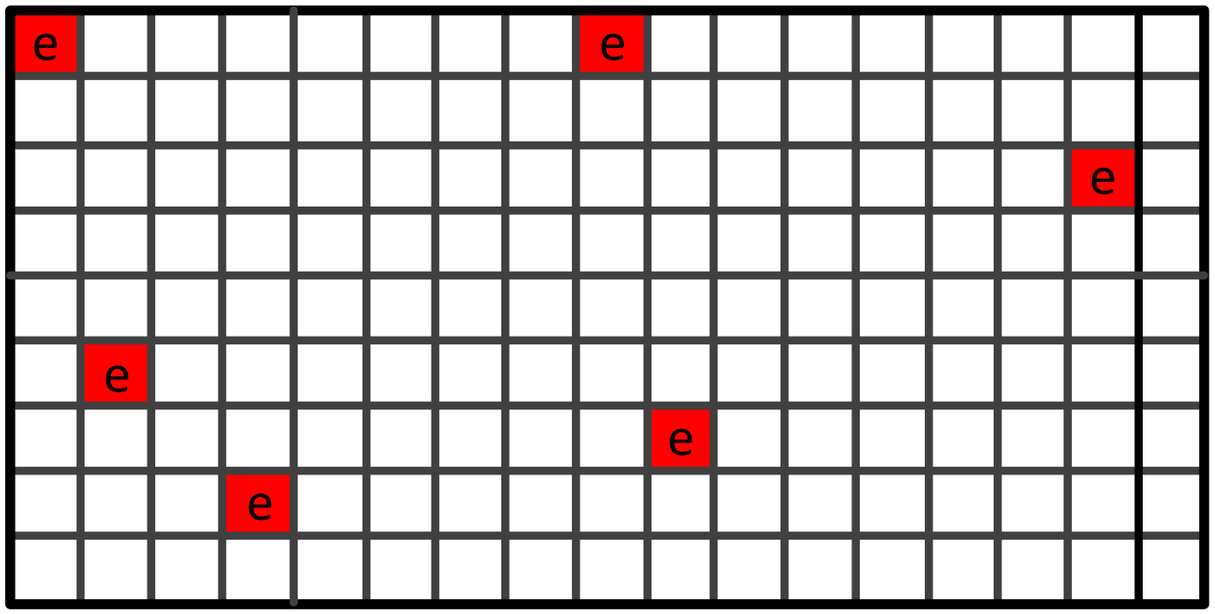

$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

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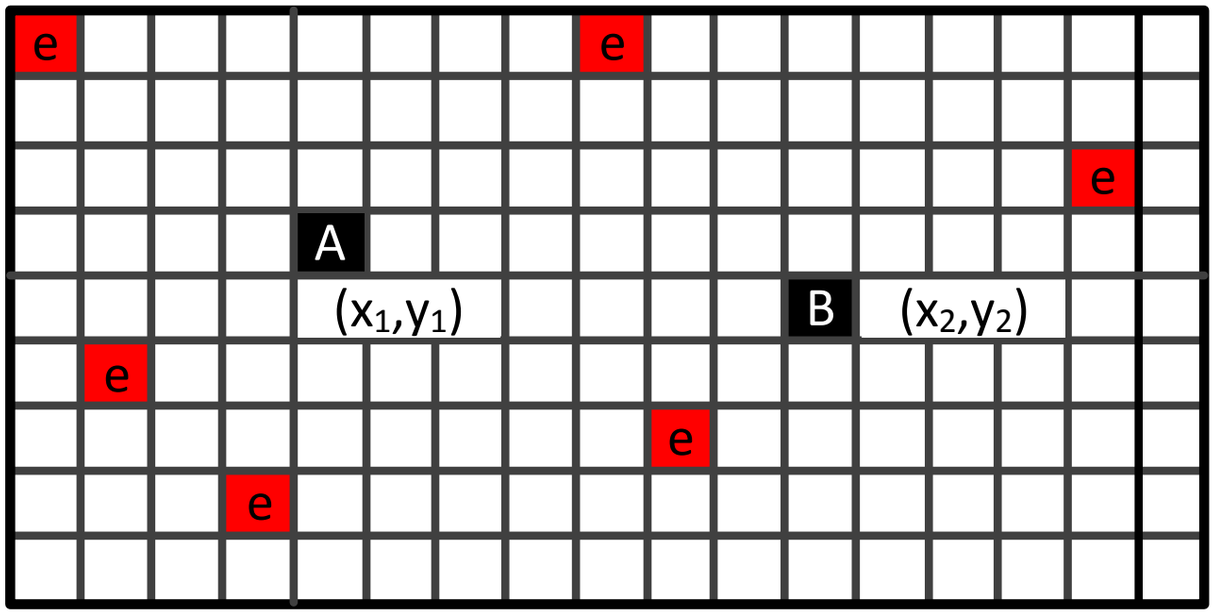
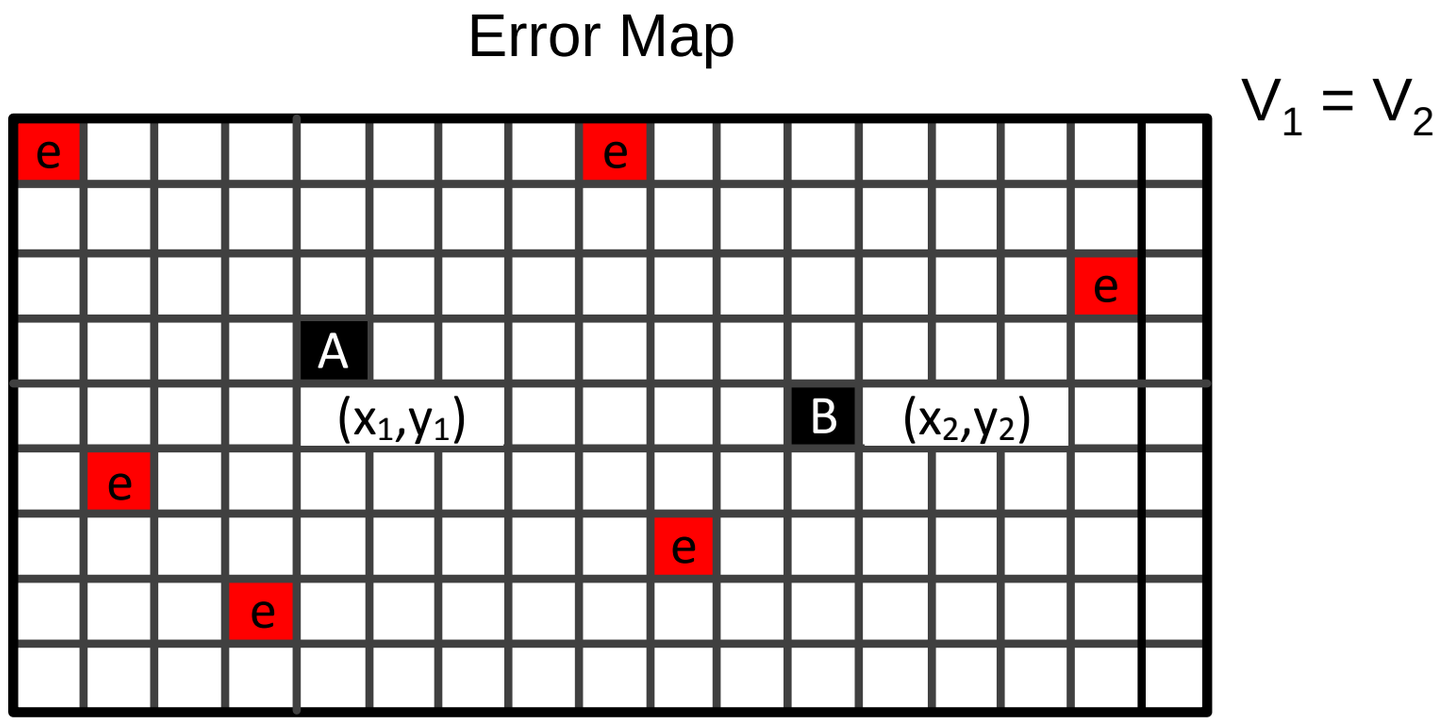


$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

Challenge and Response

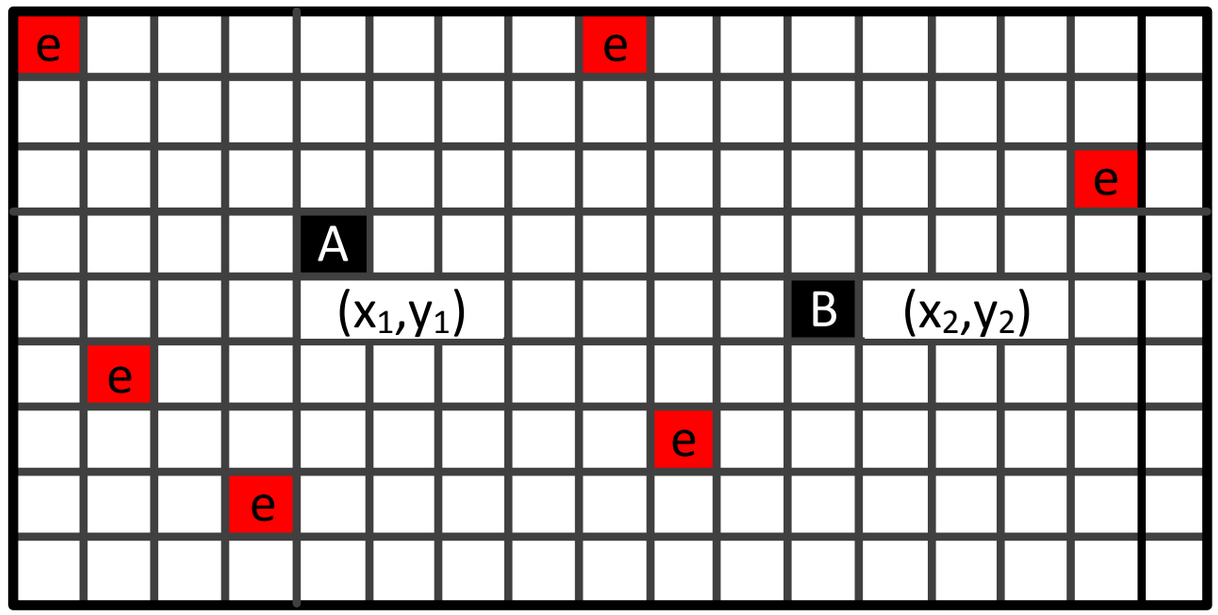


$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

Challenge and Response

Error Map

$V_1 = V_2$



$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

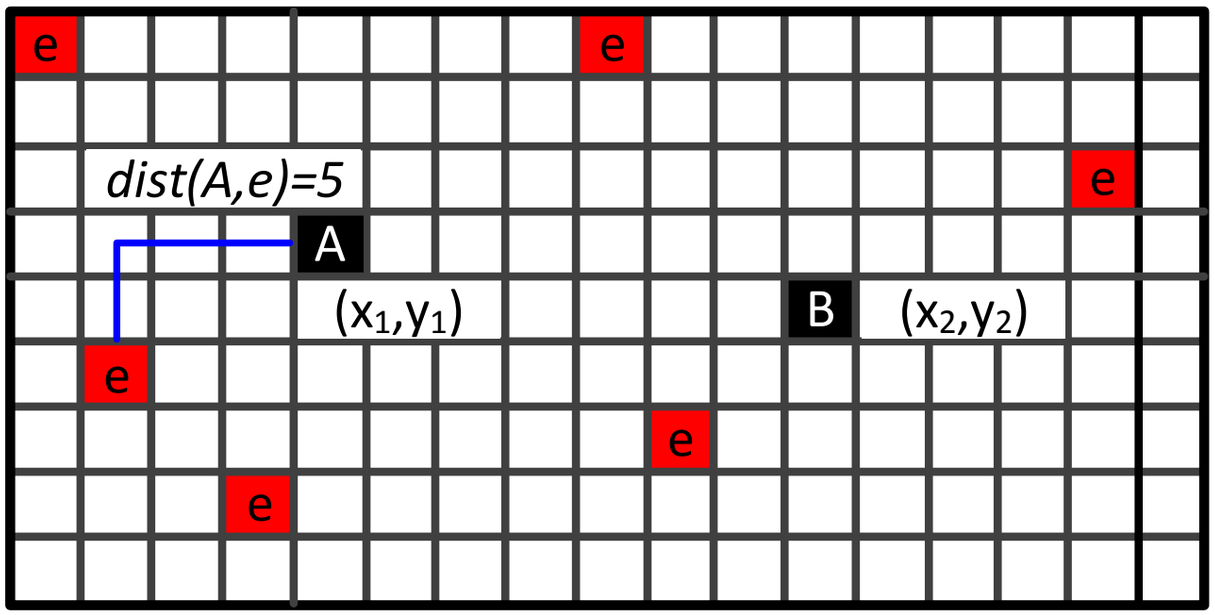
$$Response = \begin{cases} 0, dist(A, e_a) < dist(B, e_b) \\ 1, dist(A, e_a) \geq dist(B, e_b) \end{cases}$$

Manhattan Distance

Challenge and Response

Error Map

$V_1 = V_2$



$$Challenge = \underbrace{(x_1, y_1}_{A}, V_1), \underbrace{(x_2, y_2}_{B}, V_2)$$

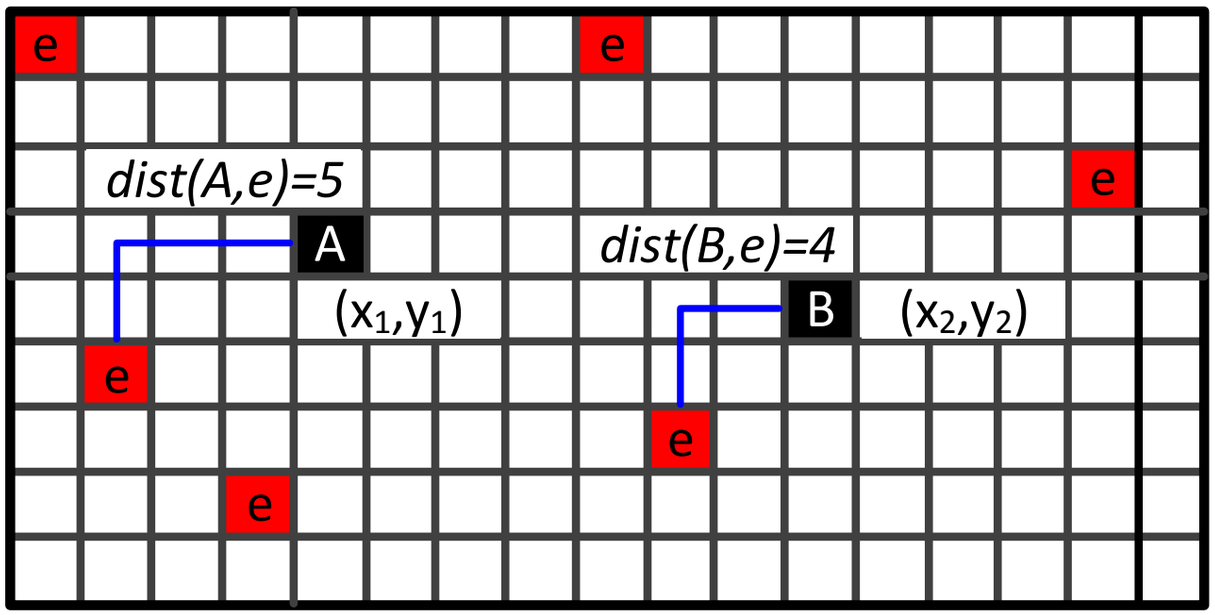
$$Response = \begin{cases} 0, dist(A, e_a) < dist(B, e_b) \\ 1, dist(A, e_a) \geq dist(B, e_b) \end{cases}$$

Manhattan Distance

Challenge and Response

Error Map

$V_1 = V_2$



$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

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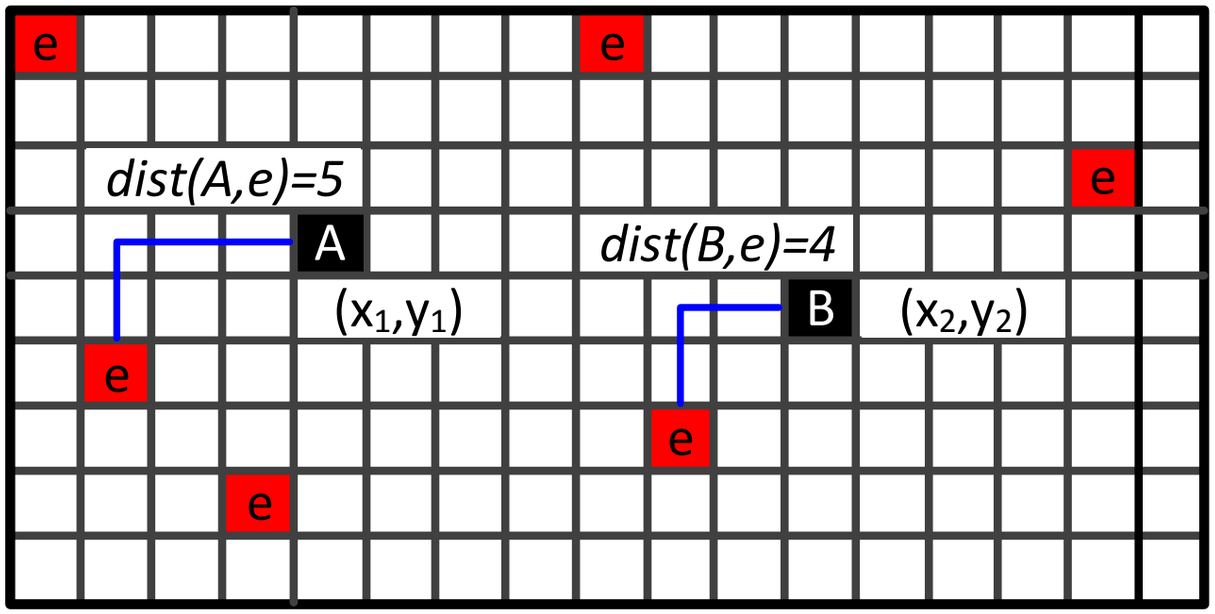
Manhattan Distance

Challenge and Response

5 > 4

Error Map

$V_1 = V_2$



$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

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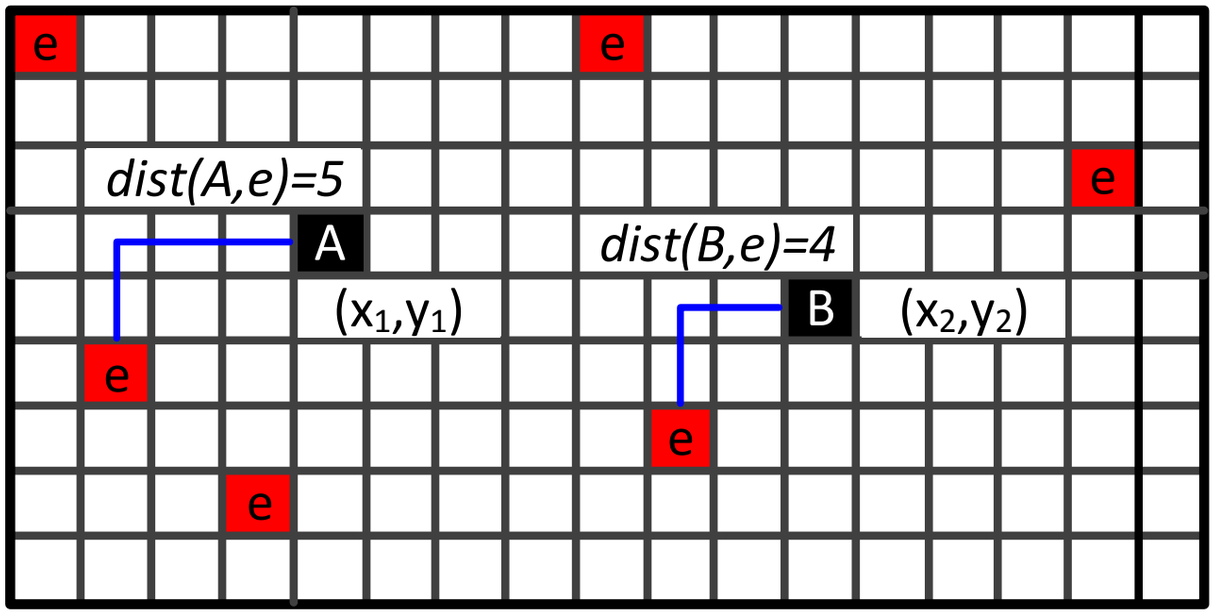
Manhattan Distance

Challenge and Response

5 > 4

Error Map



$V_1 = V_2$

1

$$Challenge = \underbrace{(x_1, y_1, V_1)}_{A}, \underbrace{(x_2, y_2, V_2)}_{B}$$

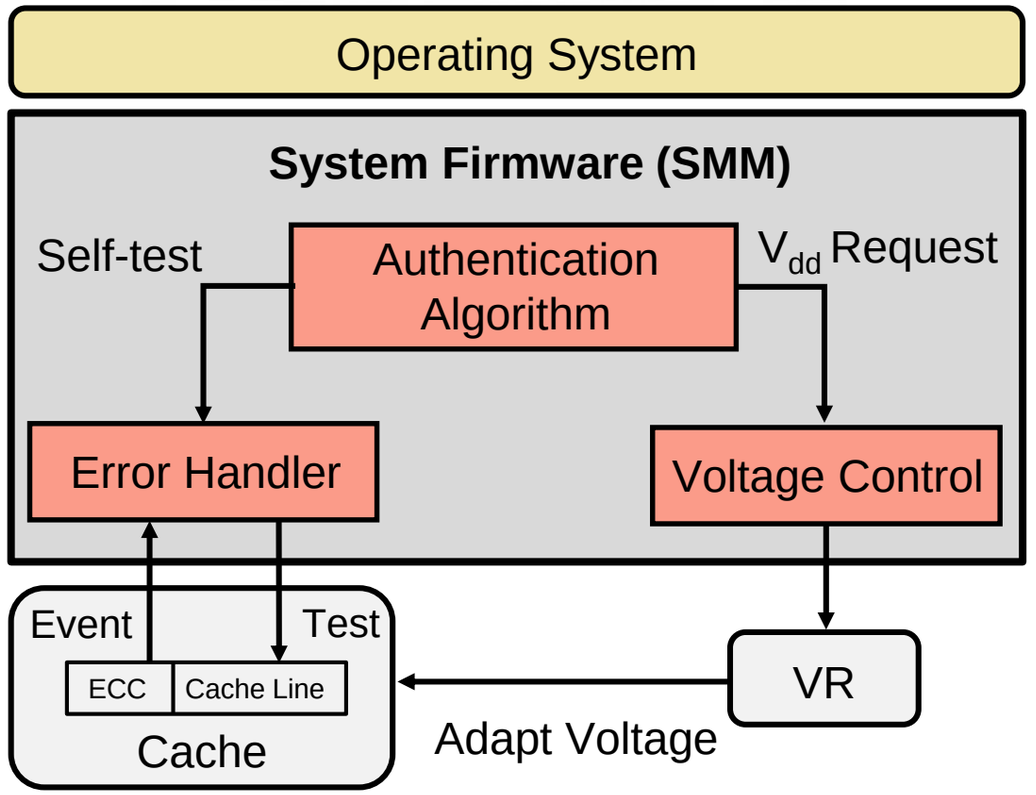
$$Response = \begin{cases} 0, dist(A, e_a) < dist(B, e_b) \\ 1, dist(A, e_a) \geq dist(B, e_b) \end{cases}$$

Manhattan Distance

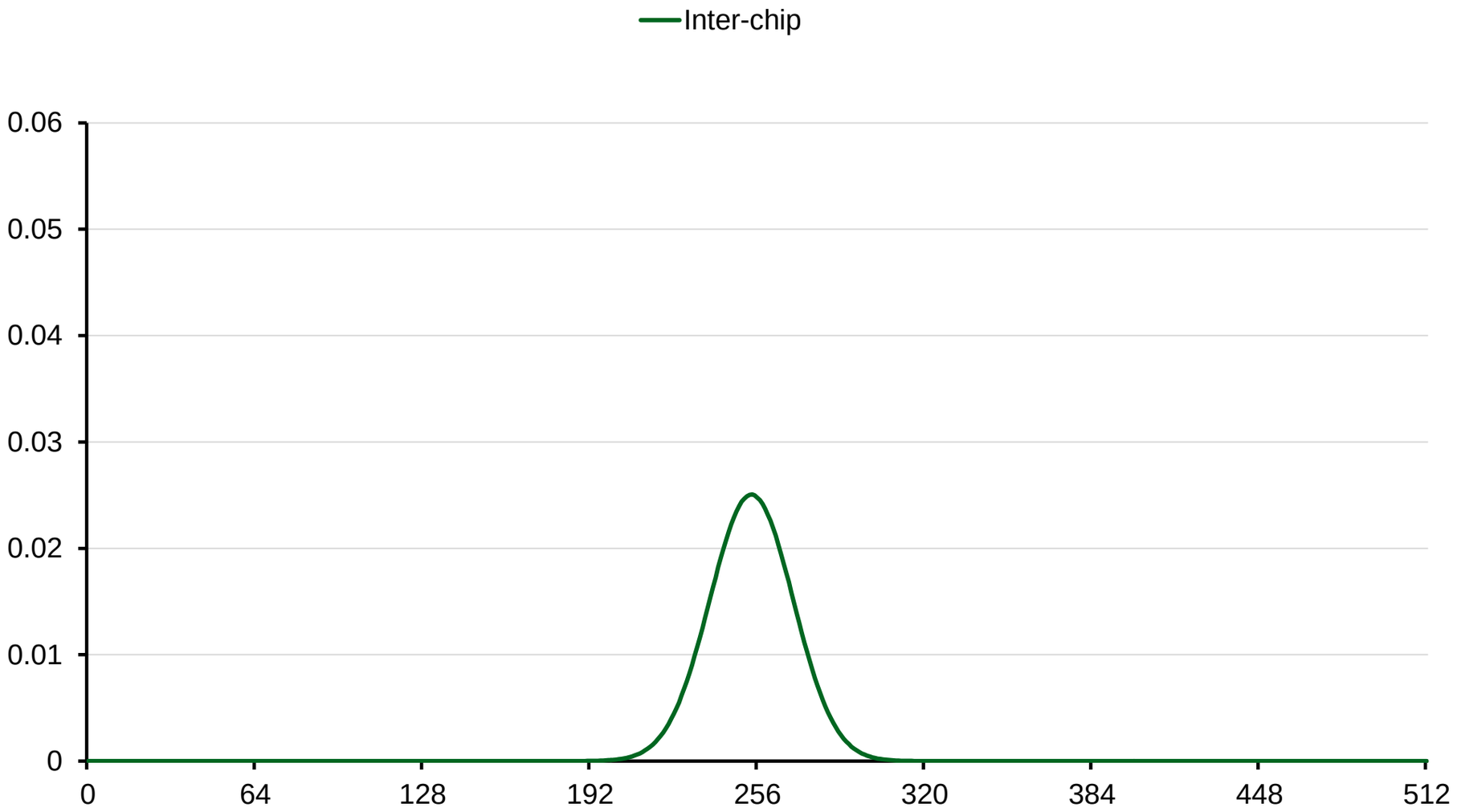
Experimental Framework

- System:
  - BL860c-i4 Integrity Server from HP
  - 2x 9560 Itanium II CPUs

- Prototype in System Firmware
  - Thermal experiments through power virus
- Monte Carlo simulations
  - Different cache sizes
  - Different error maps and noise profiles

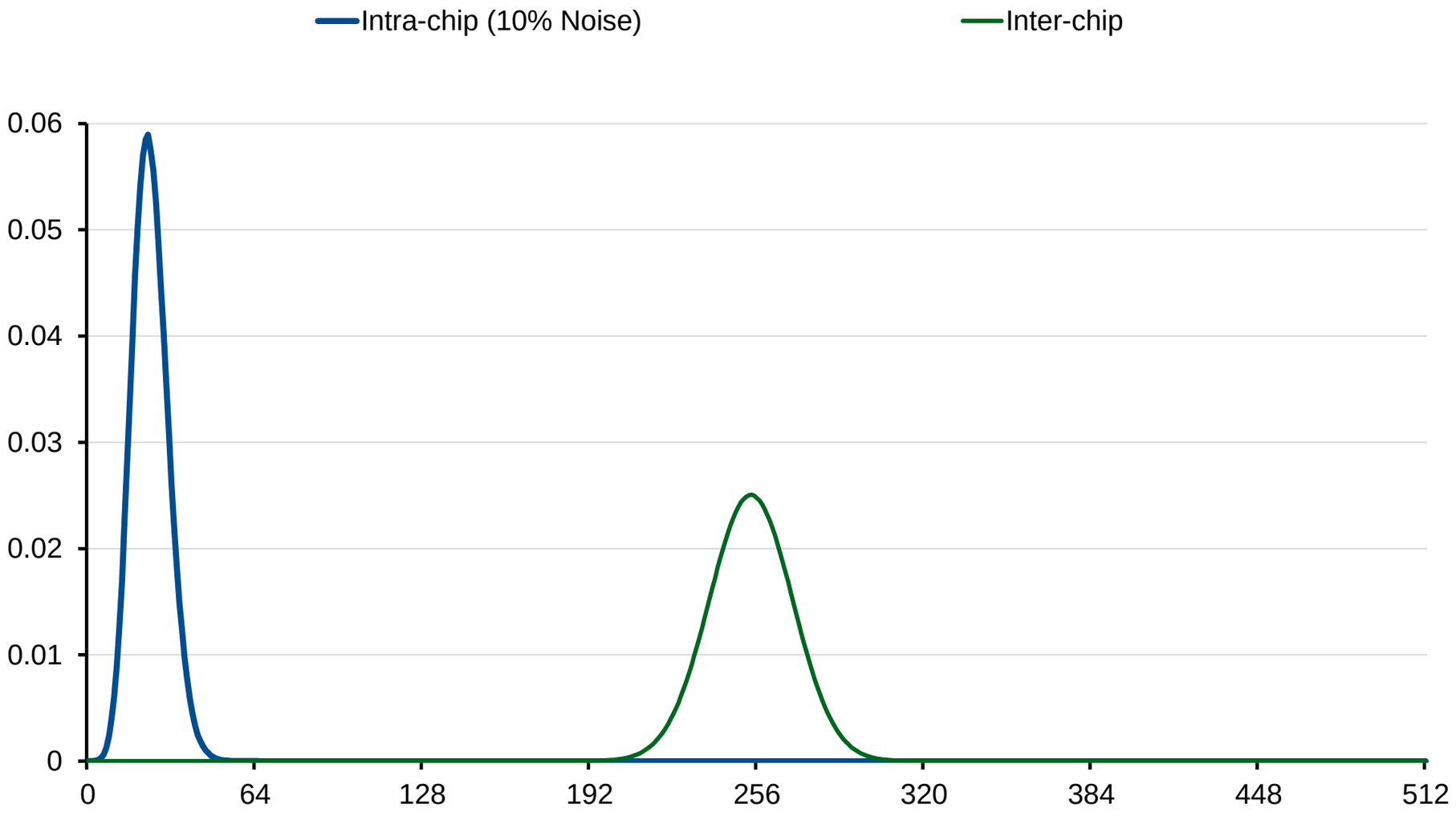


Identification and Noise



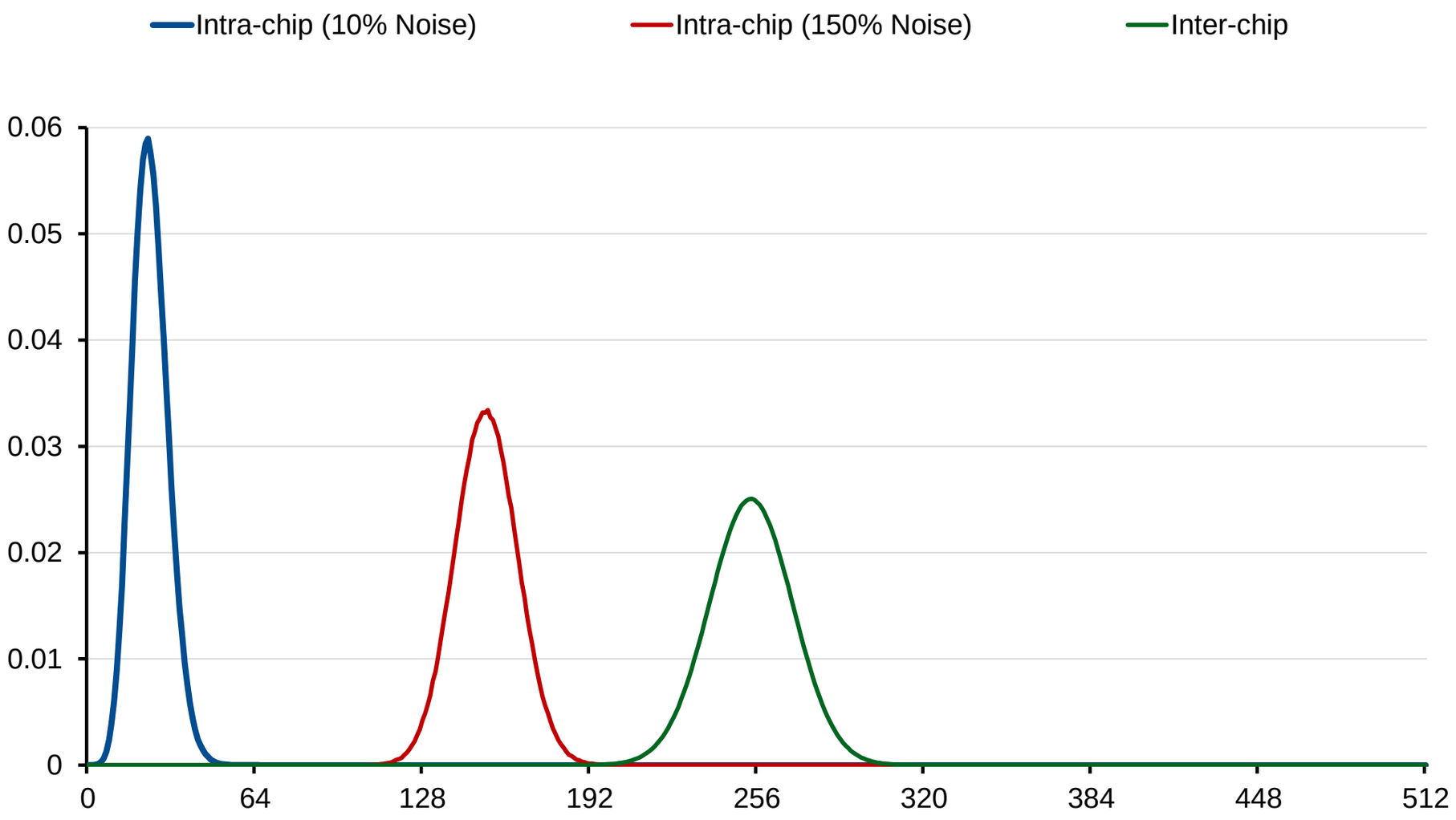
Identification in presence of environmental and measurement noise

Identification and Noise



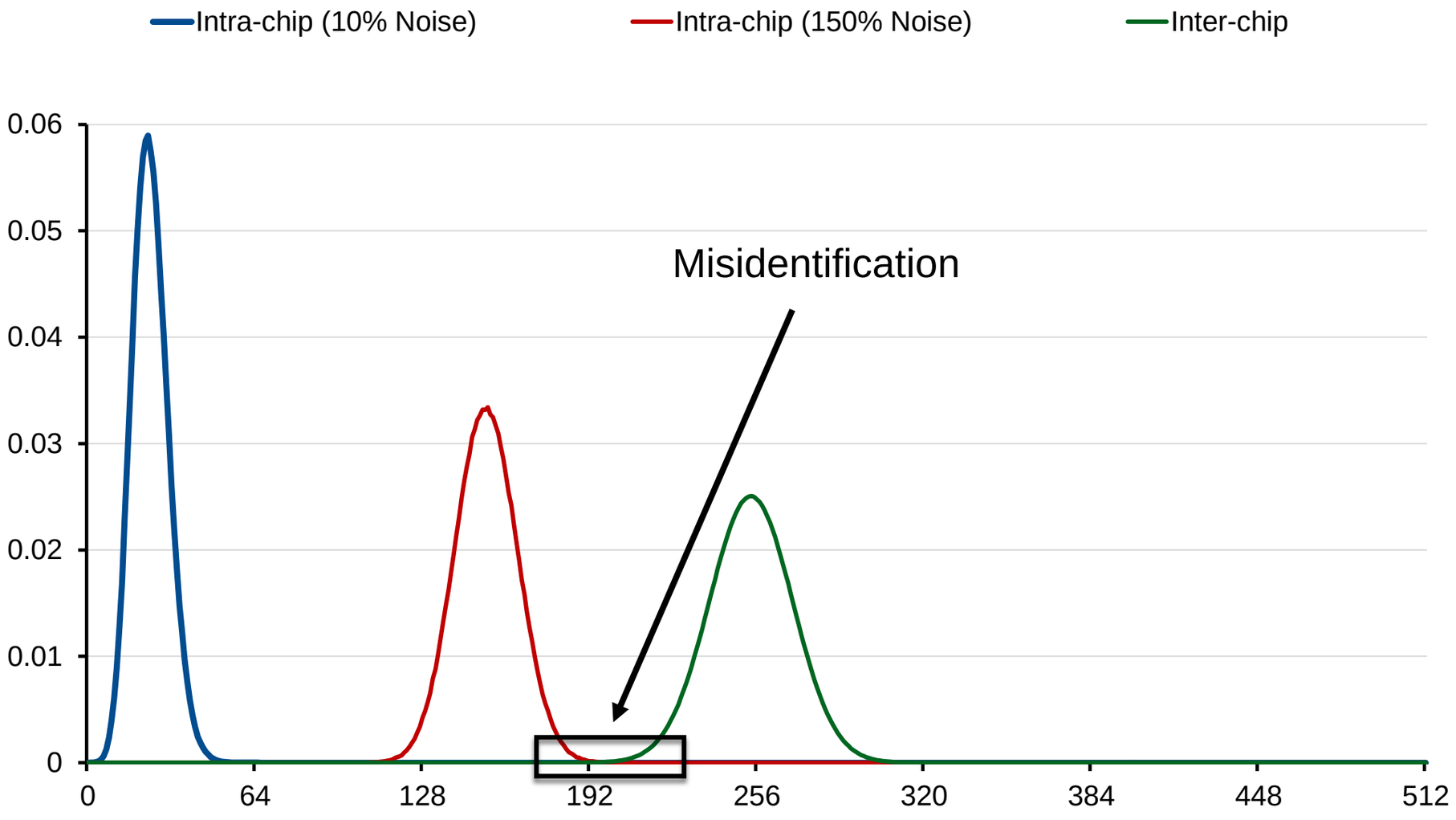
Identification in presence of environmental and measurement noise

Identification and Noise



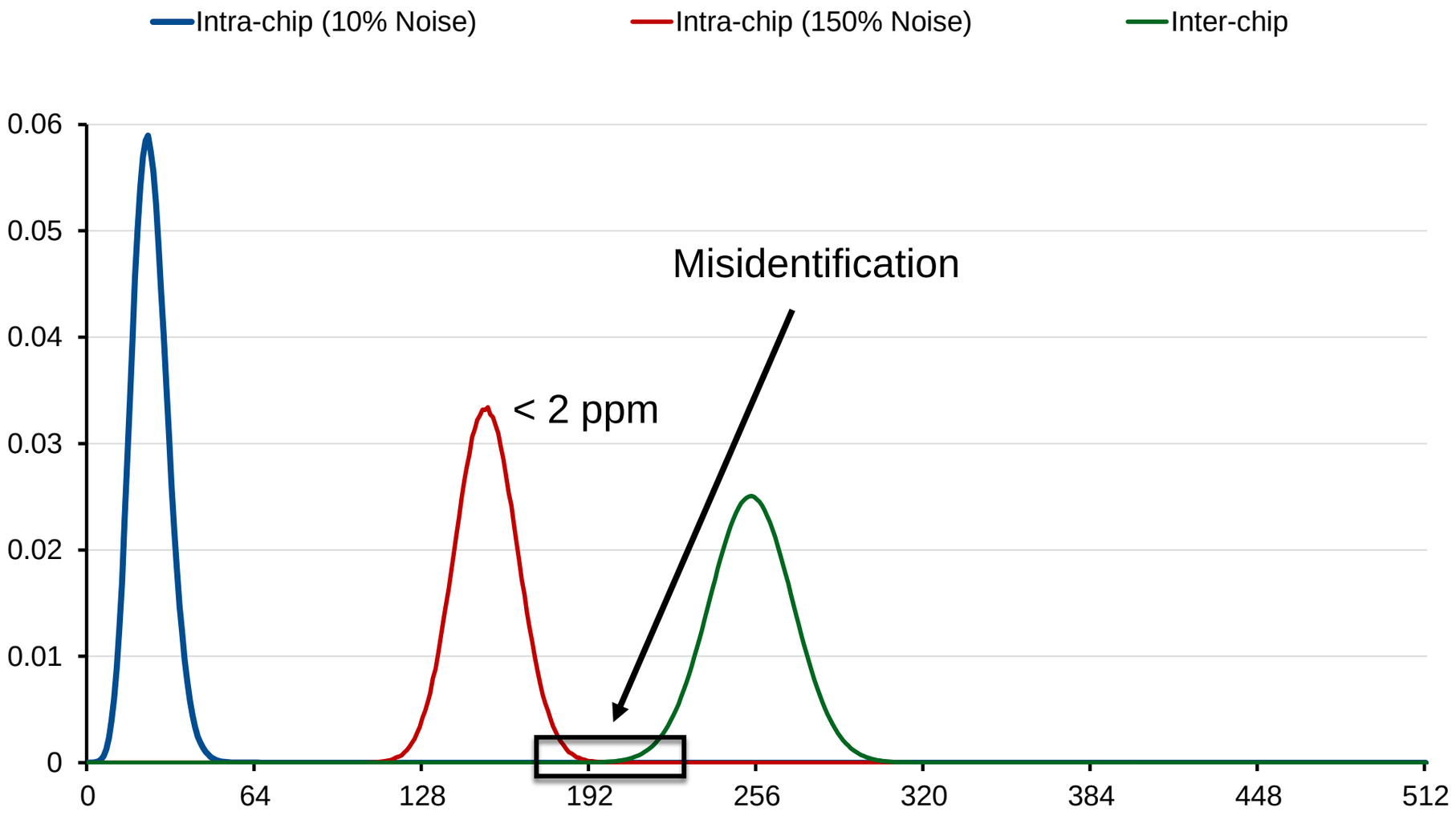
Identification in presence of environmental and measurement noise

Identification and Noise



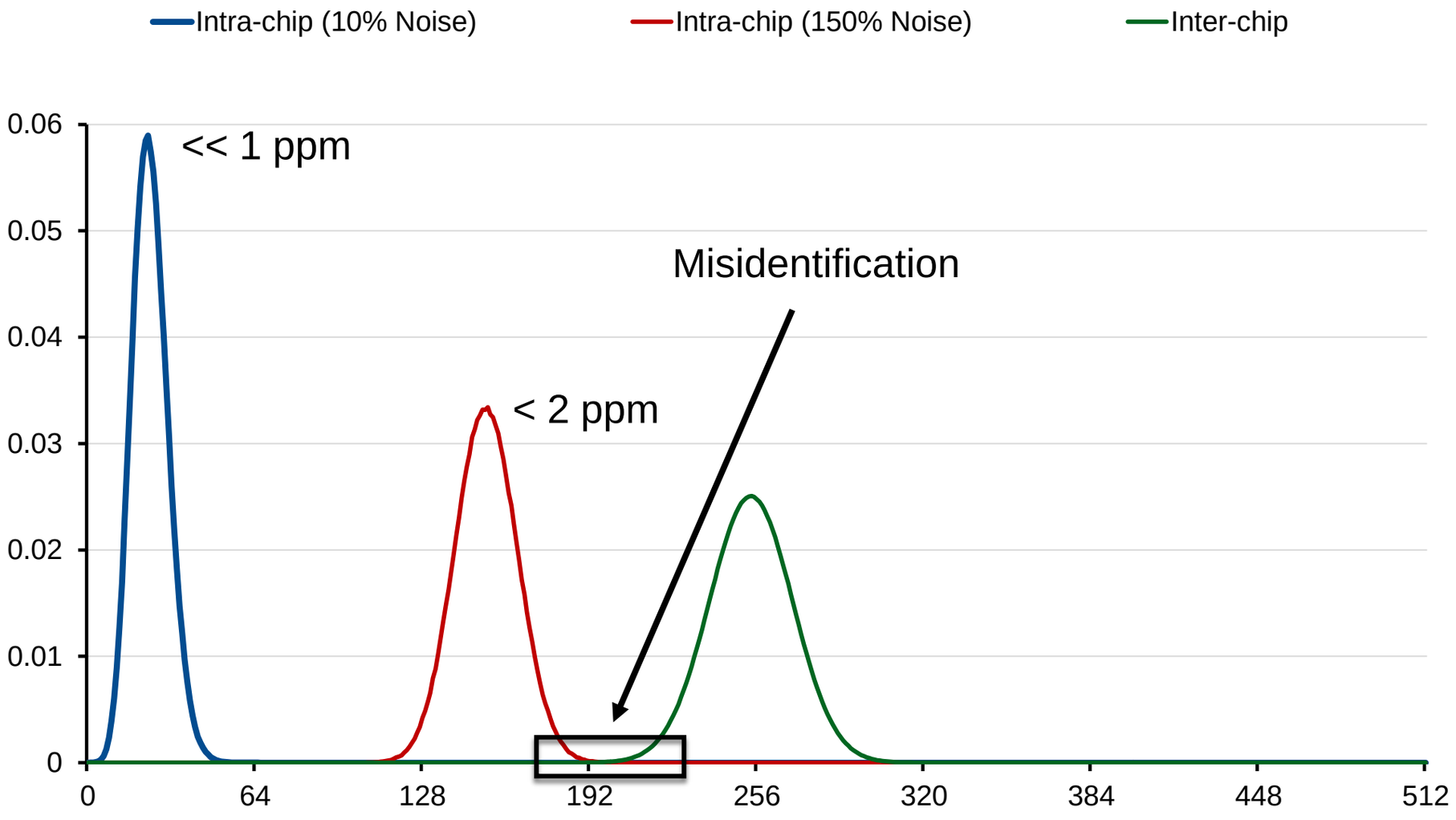
Identification in presence of environmental and measurement noise

Identification and Noise



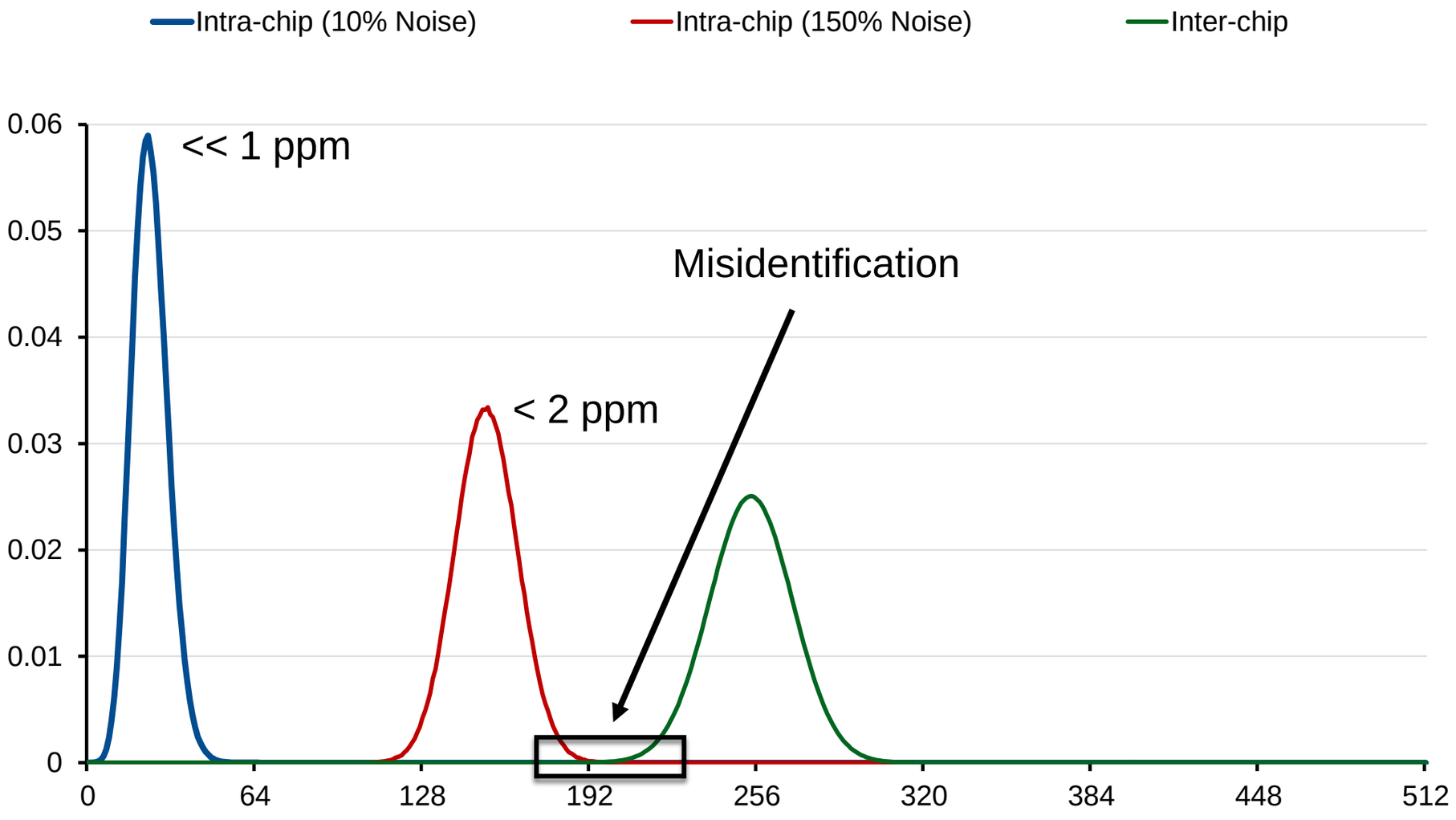
Identification in presence of environmental and measurement noise

Identification and Noise



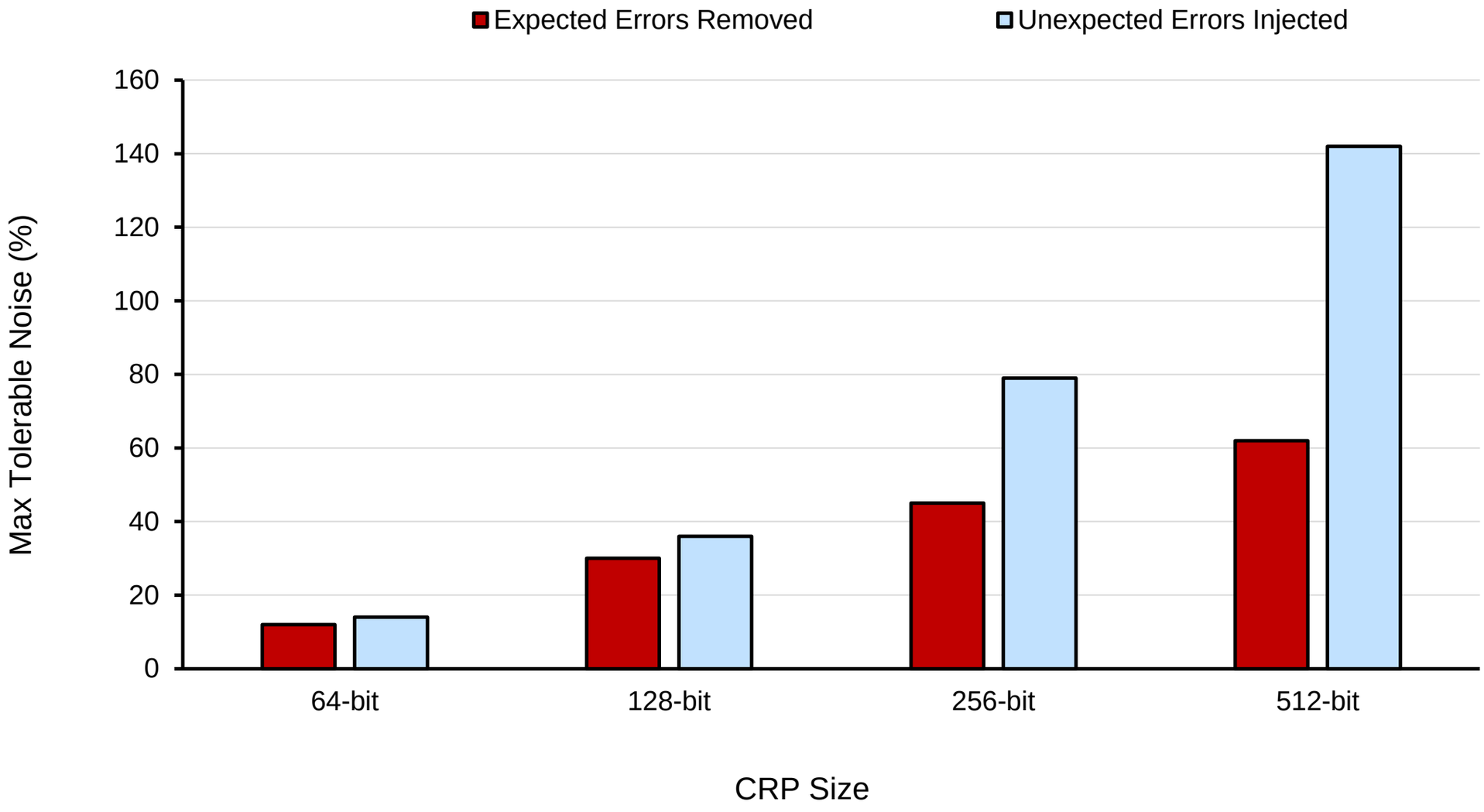
Identification in presence of environmental and measurement noise

Identification and Noise

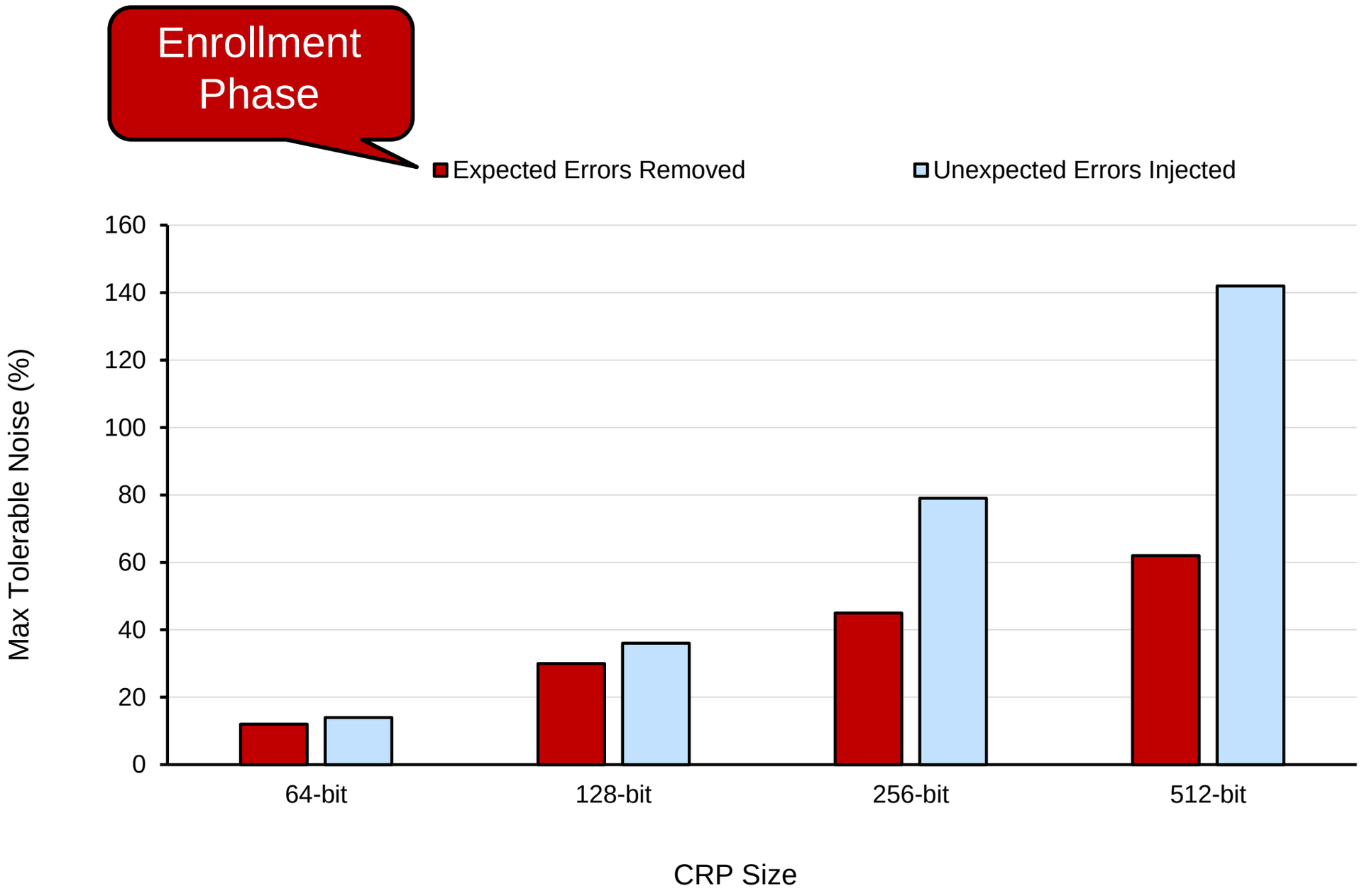


Observe 6% intra-chip variation after +25° C

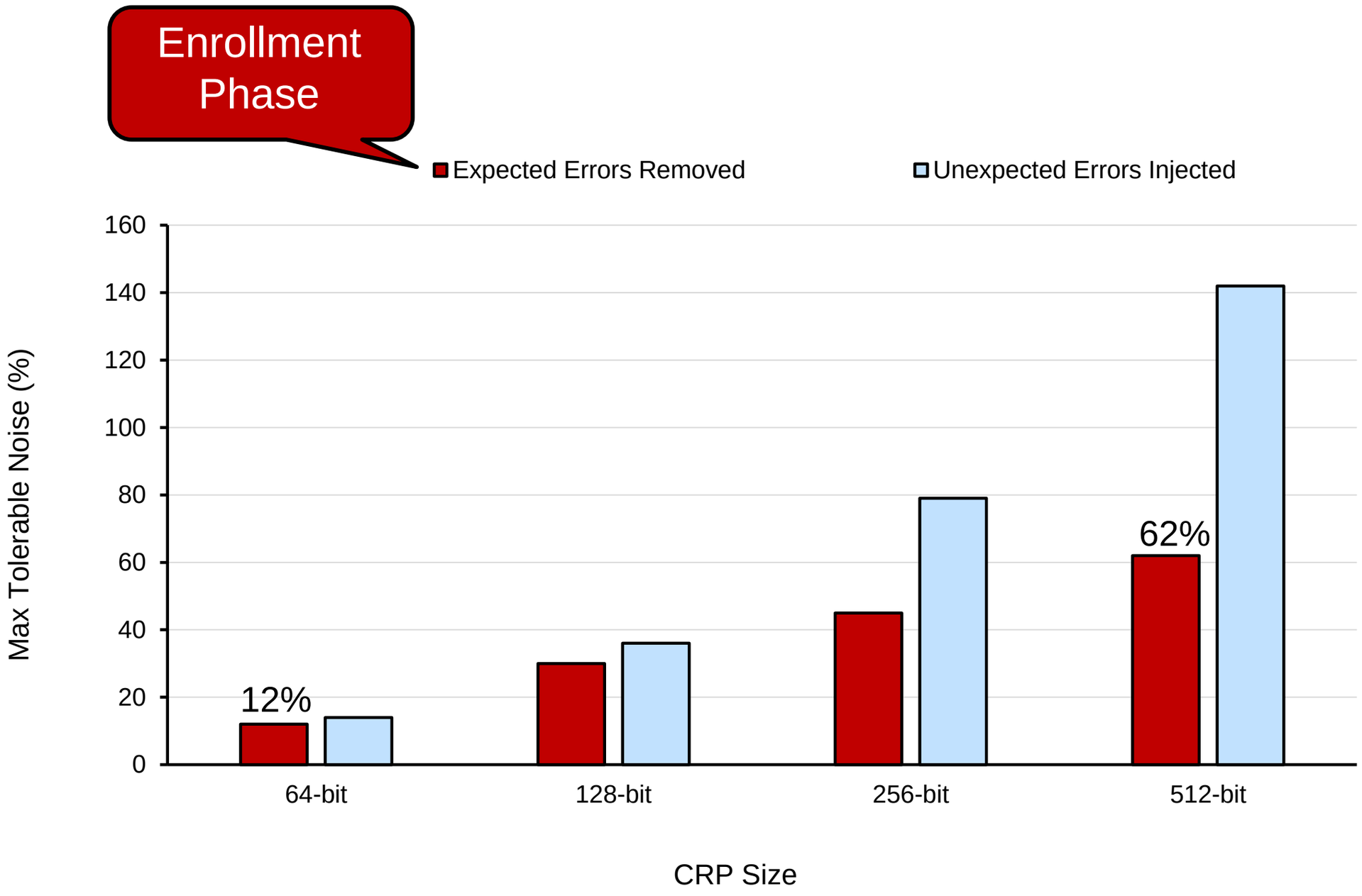
Resiliency to Noise



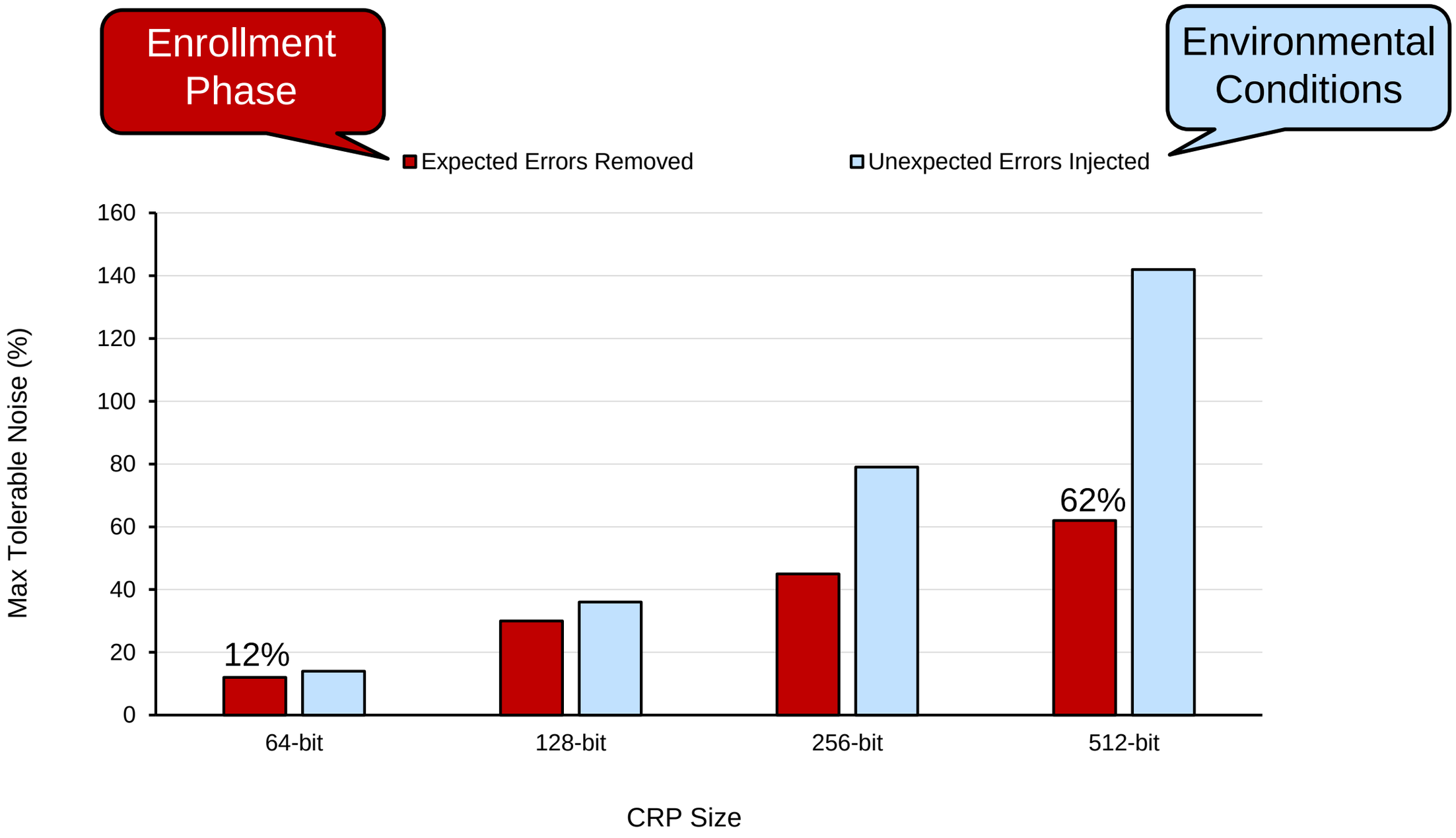
Resiliency to Noise



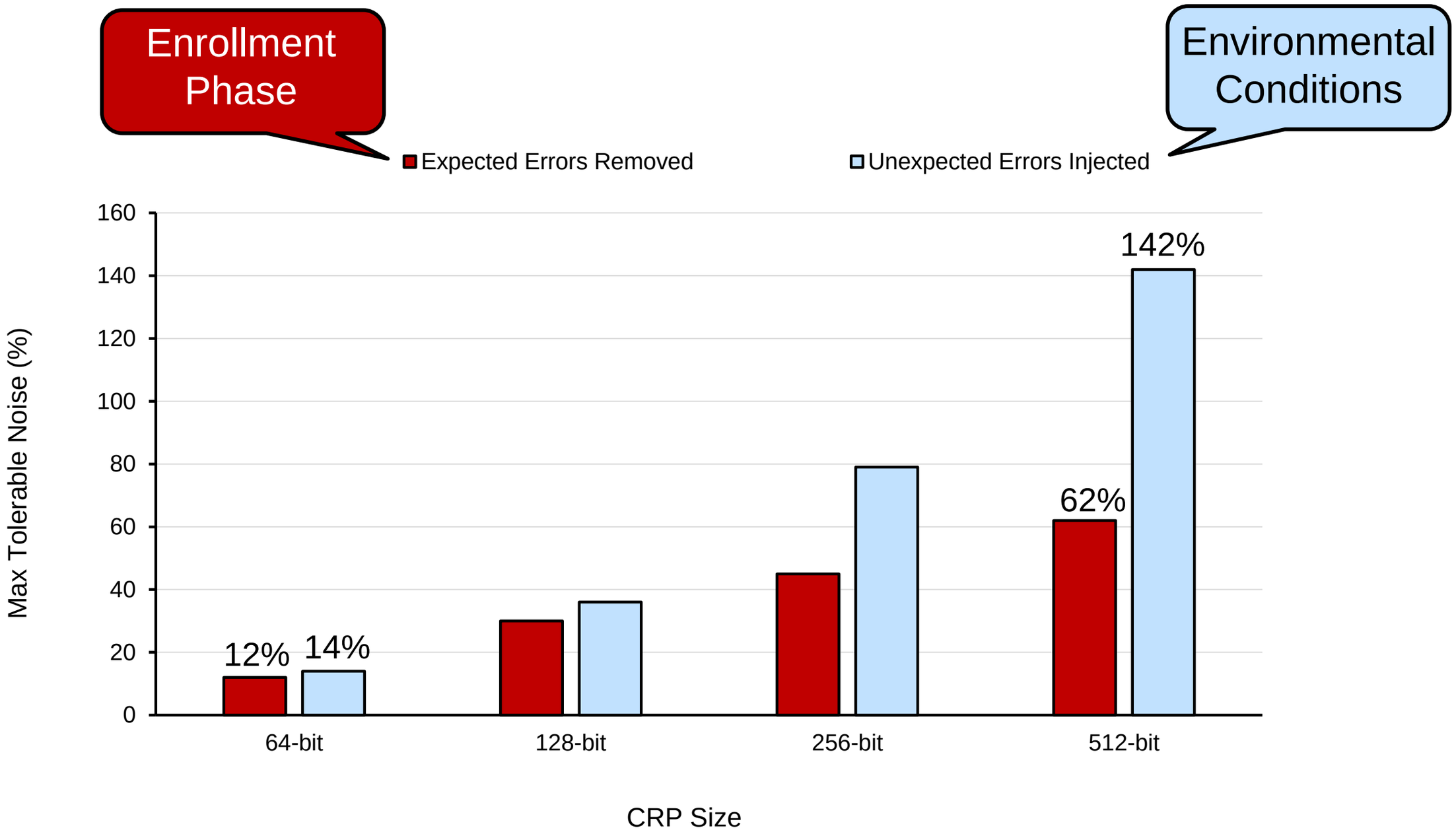
Resiliency to Noise



Resiliency to Noise



Resiliency to Noise



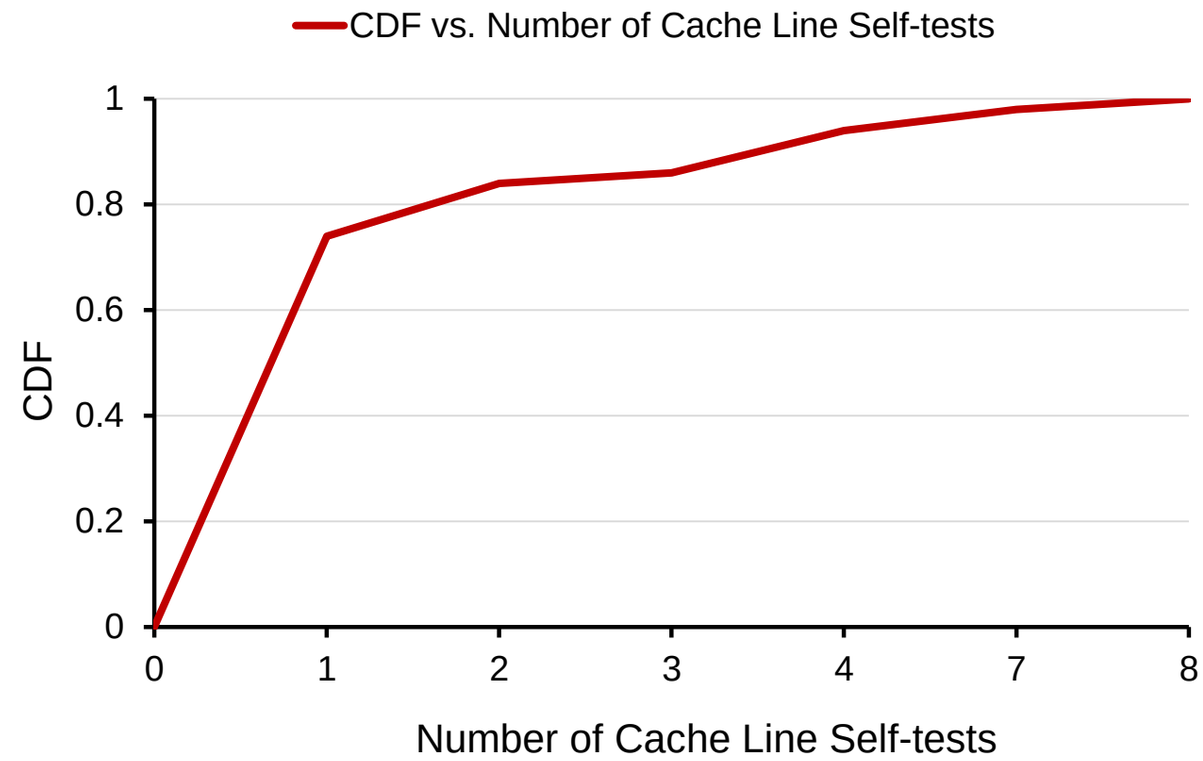
Repeatability and Performance

Repeatability and Performance

- Repeatable cache line errors

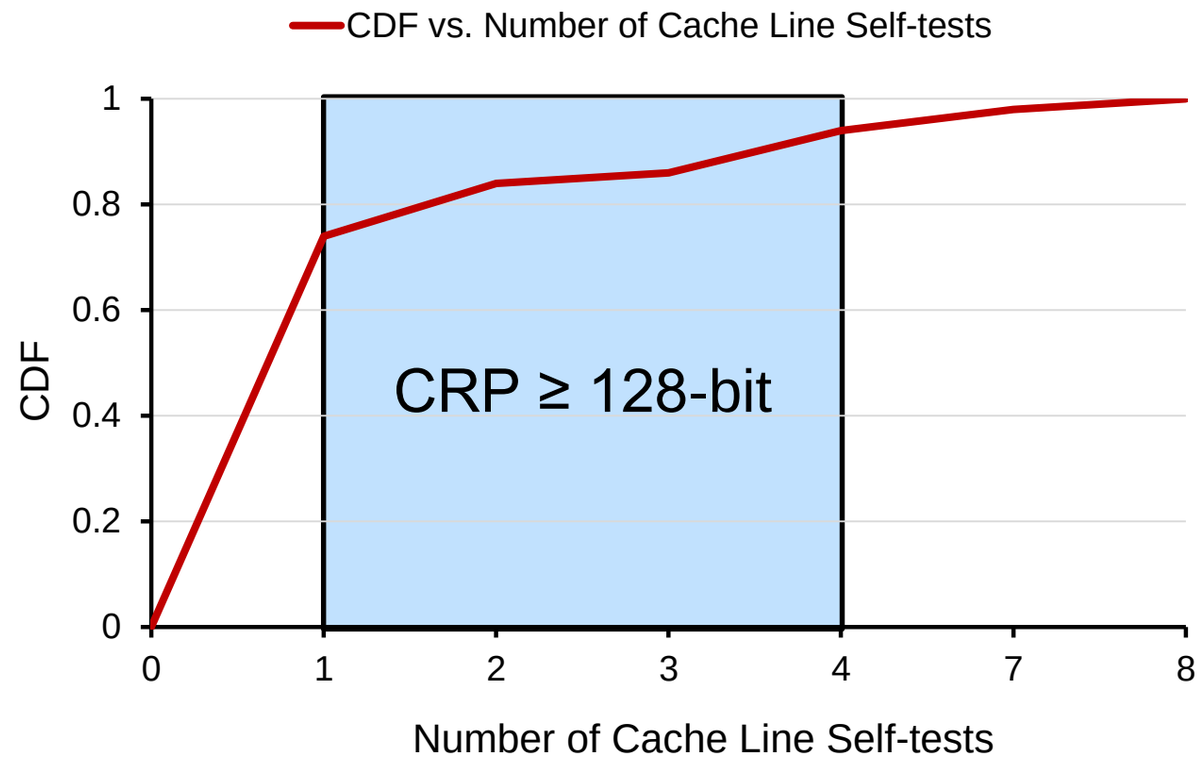
Repeatability and Performance

- Repeatable cache line errors



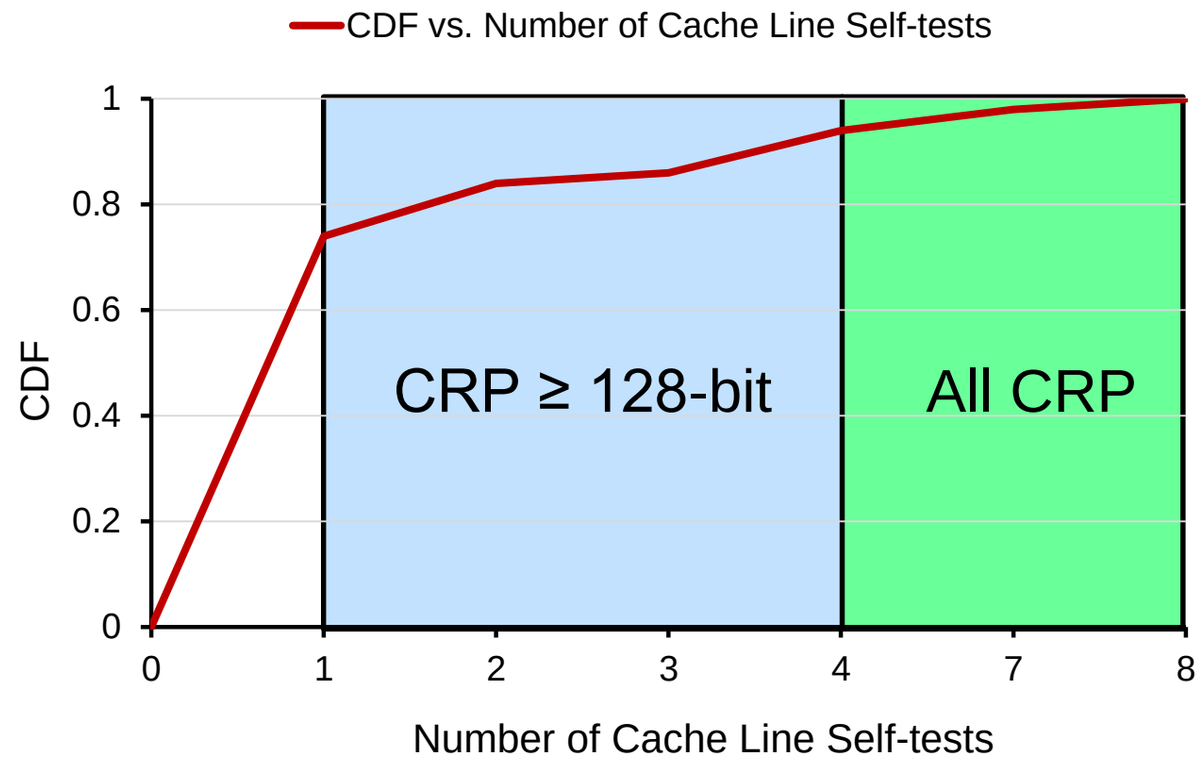
Repeatability and Performance

- Repeatable cache line errors



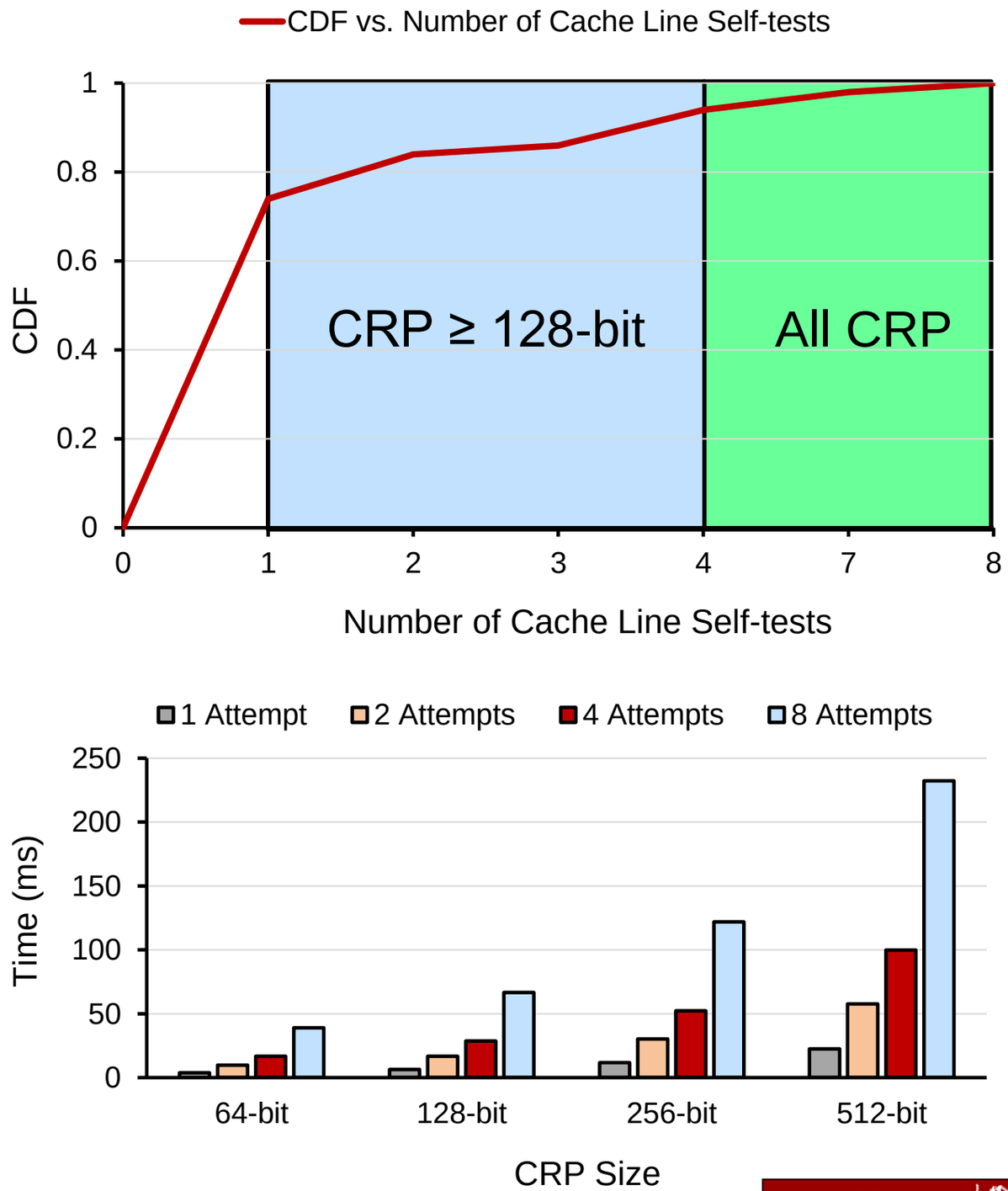
Repeatability and Performance

- Repeatable cache line errors



Repeatability and Performance

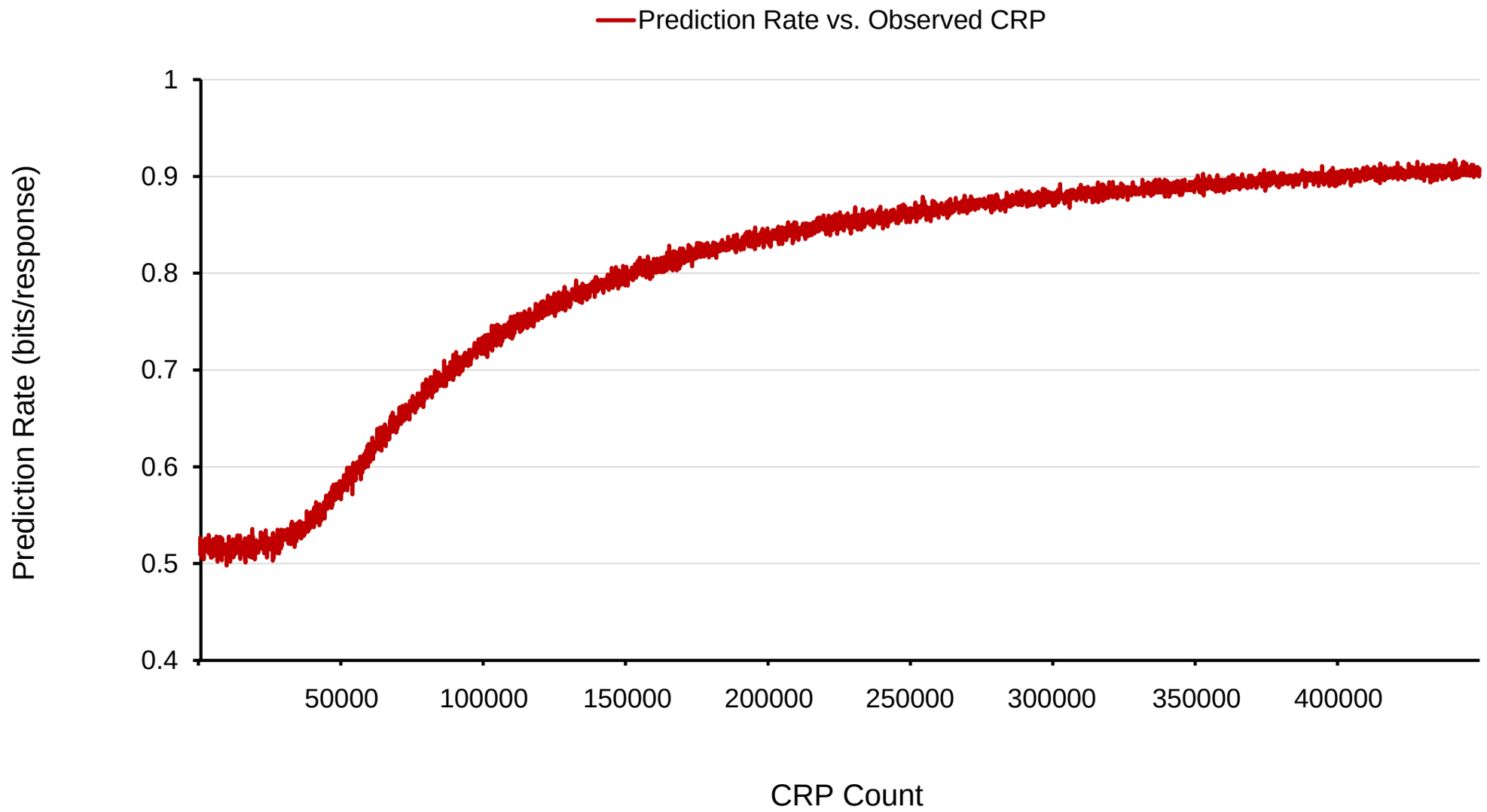
- Repeatable cache line errors



- Linear increase in runtime as a function of self-test attempts

Model Building Attack Case Study

Model Building Attack Case Study



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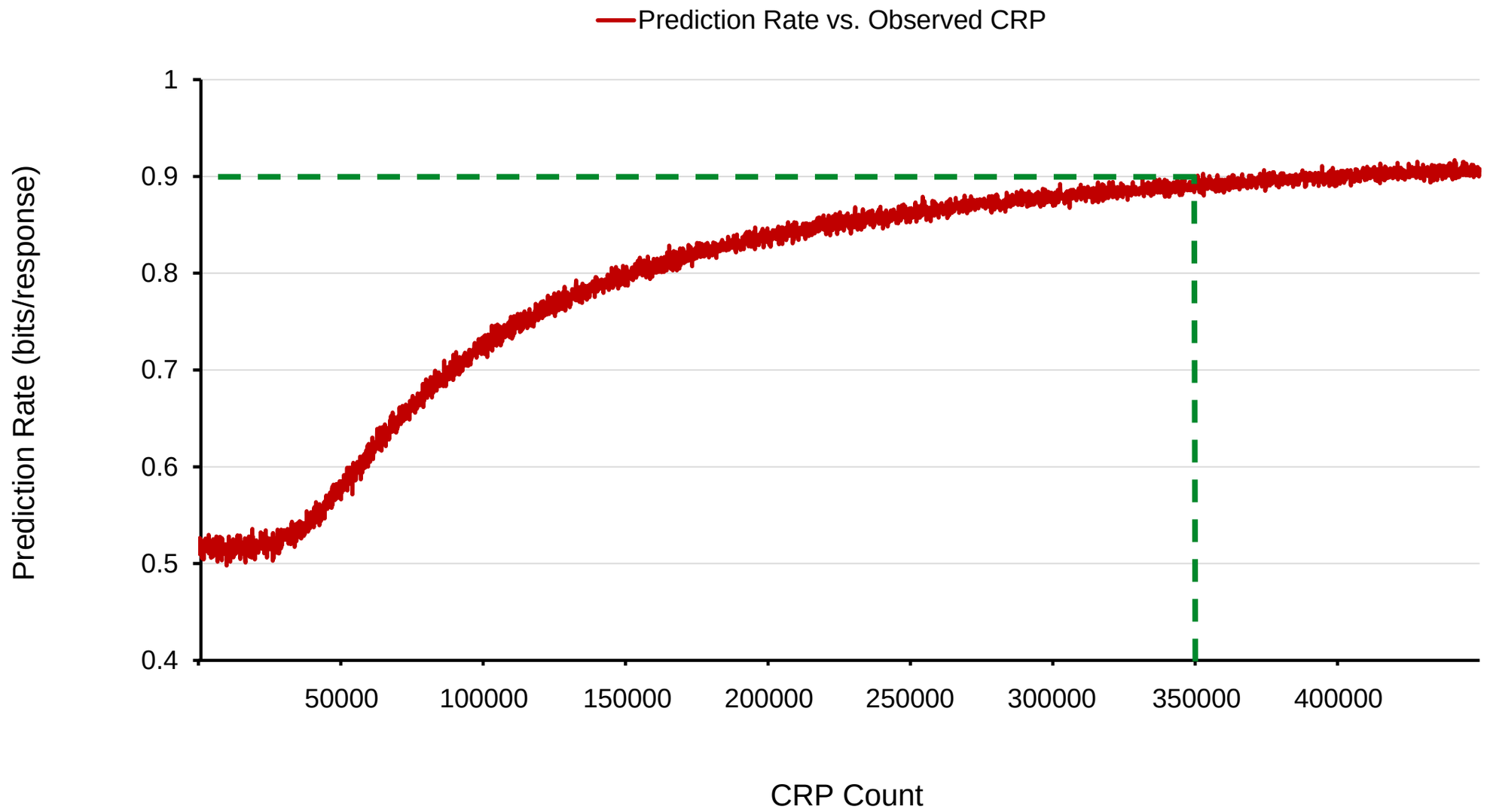
Model Building Attack Case Study



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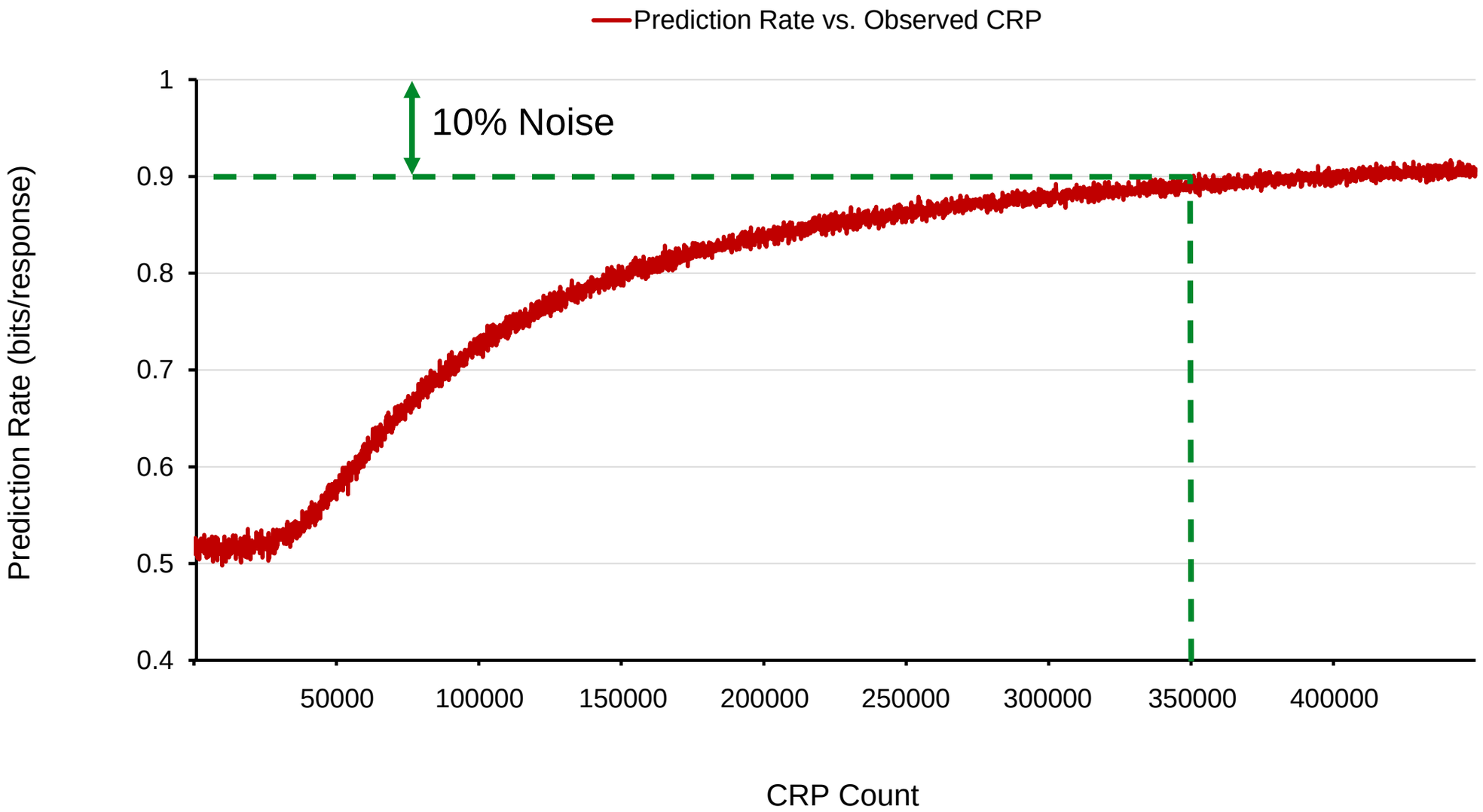
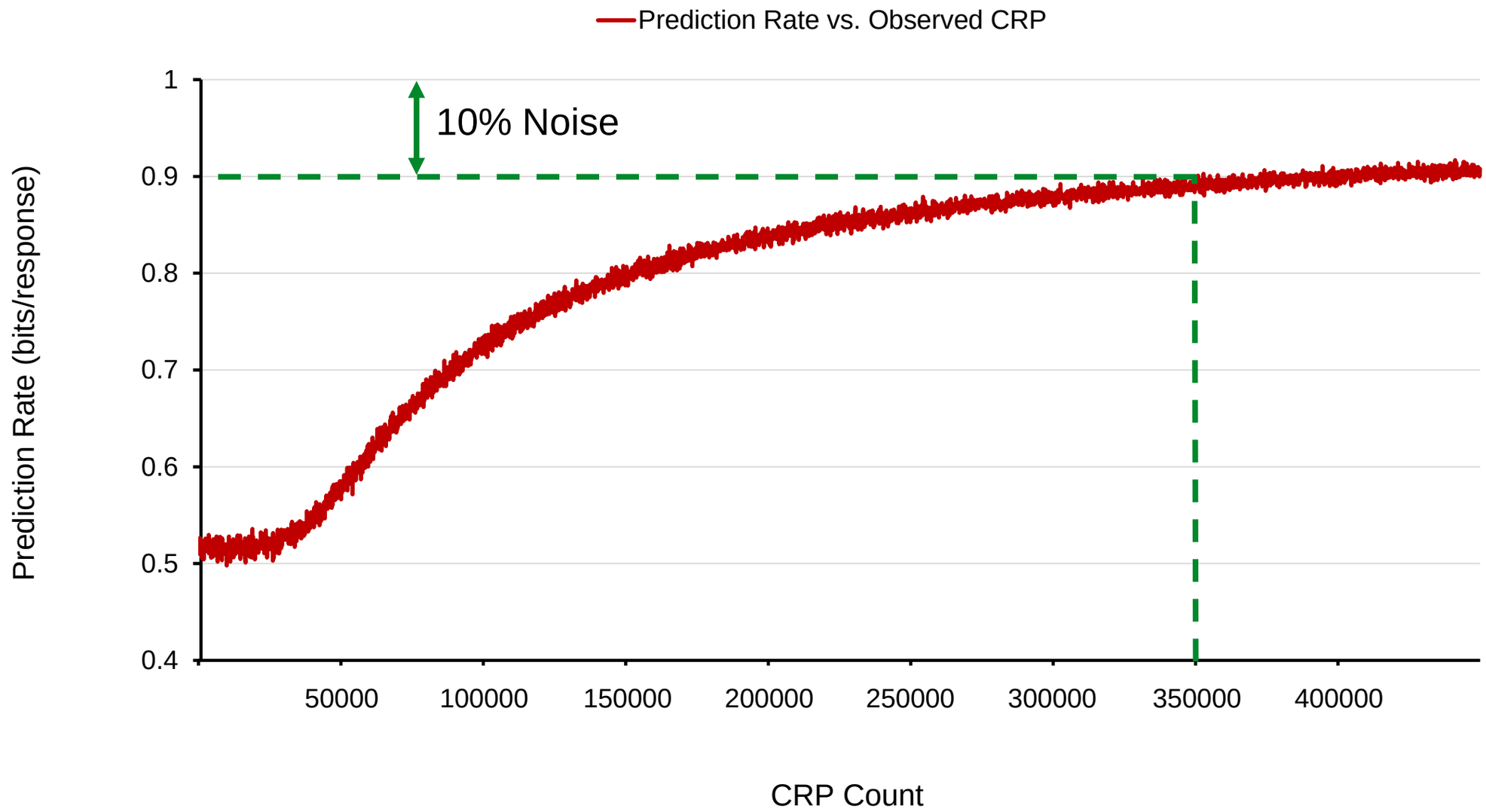
Model Building Attack Case Study



Model Building Attack Case Study



Regenerate logical error map

Conclusion

- Observe that correctable errors in caches can be used as silicon fingerprints
- Introduce a challenge-response design that can sustain large number of authentications (10 year lifetime)
- Demonstrate robustness of technique to noise (up to 142%)
- Realize a proof-of-concept to show system is practical

Thank you!

Questions?

Authenticache: Harnessing Cache ECC for System Authentication

Anys Bacha and Radu Teodorescu

Department of Computer Science and Engineering

The Ohio State University

http://arch.cse.ohio-state.edu

THE OHIO STATE UNIVERSITY

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