Using ECC Feedback to Guide Voltage Speculation in Low-Voltage Processors

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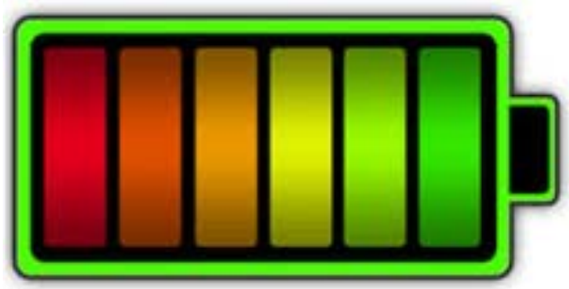
COMPUTER ARCHITECTURE RESEARCH LAB

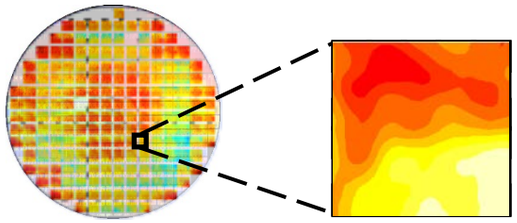
Energy Efficiency



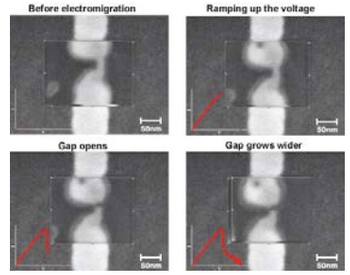
Energy efficiency is now crucial to all computing markets, especially in the growth areas: mobile and cloud computing.

Microprocessor Challenges

Process variation



Circuit aging



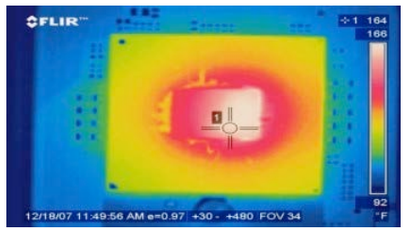
V_{dd}

nominal V_{dd}

High guardband (10-20%)

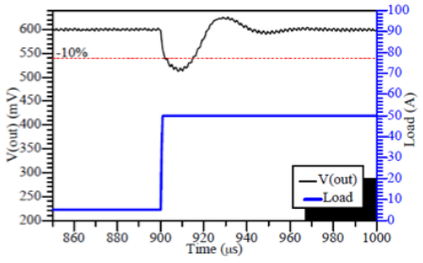
safe V_{dd}

Temperature



Energy inefficient

Voltage noise



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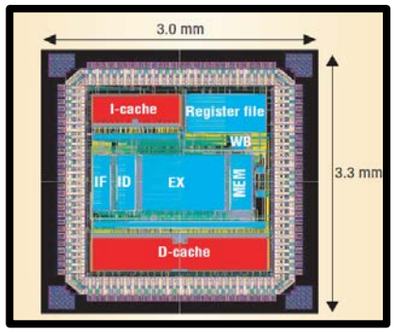
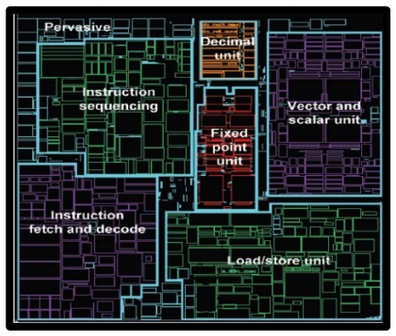
Voltage Speculation

- Razor (Ernst et al. MICRO'03)
  - Shadow latches detect/correct errors



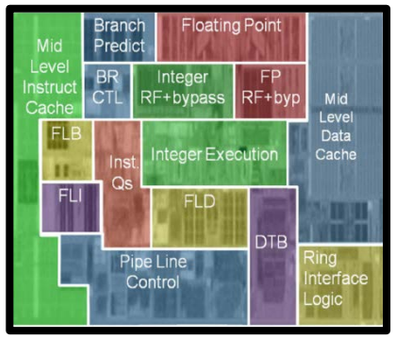
Razor

- IBM POWER7 (Lefurgy et al. MICRO'11)
  - Critical path monitors help avoid errors



POWER7

- Itanium 9560 (Bacha and Teodorescu ISCA'13)
  - ECC conservatively help avoid errors via software speculation



Itanium 9560

The Case for Low Voltage Speculation

- Commercial interest in low voltage for substantial energy savings

Intel Claremont solar chip

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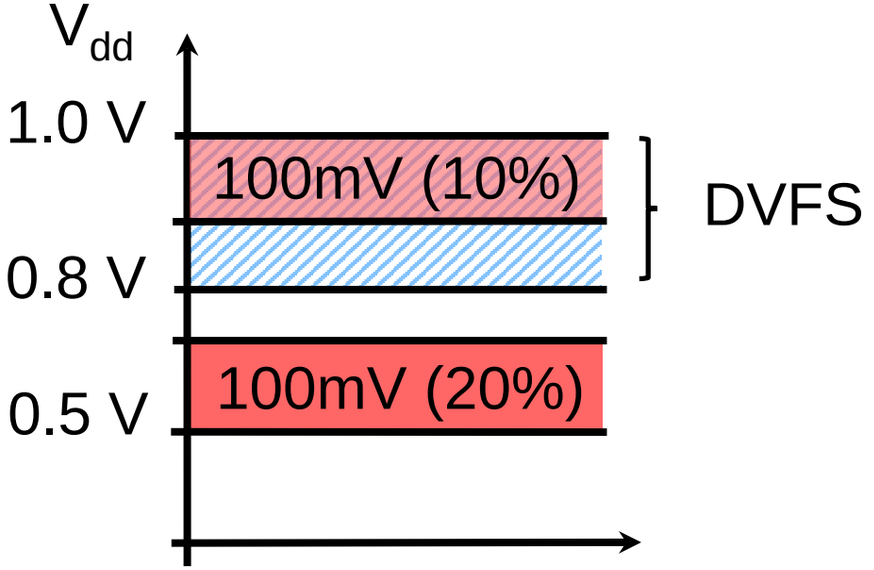
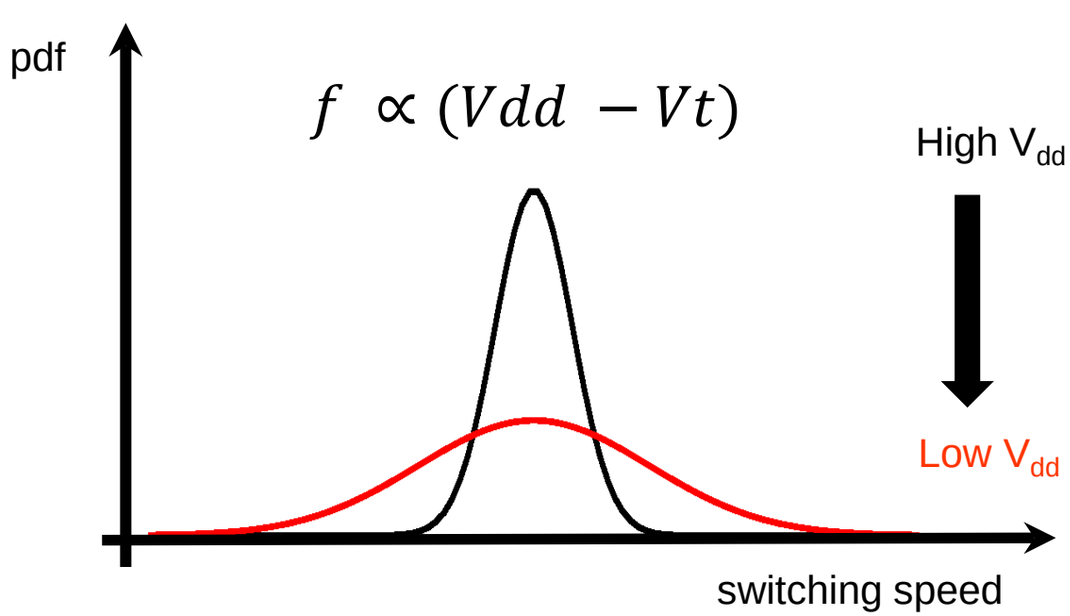


Prohibitive guardbands



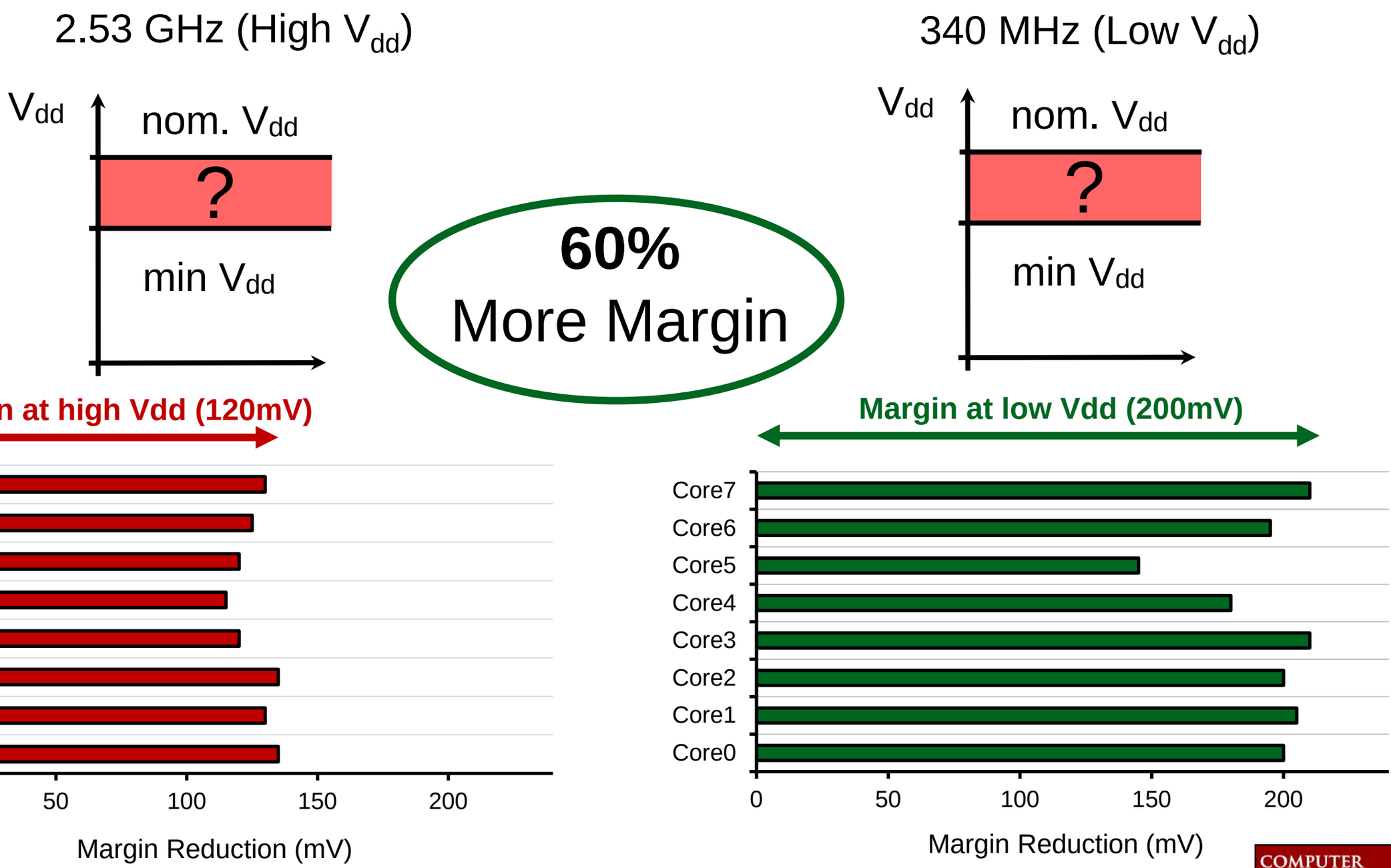
Amplified process variation effects

Outline

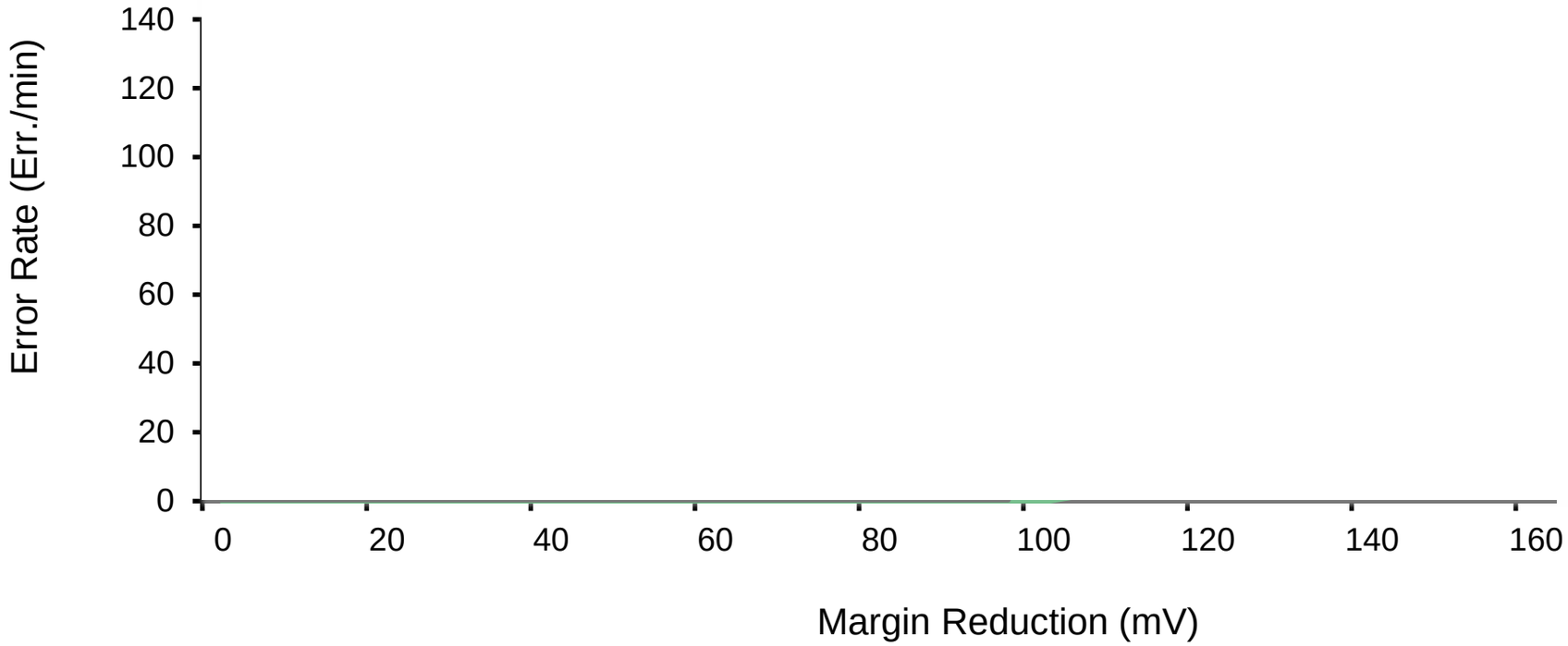
- Motivation
- ECC-based voltage speculation
- Experimental framework
- Evaluation

Margin Opportunity at Low Voltage

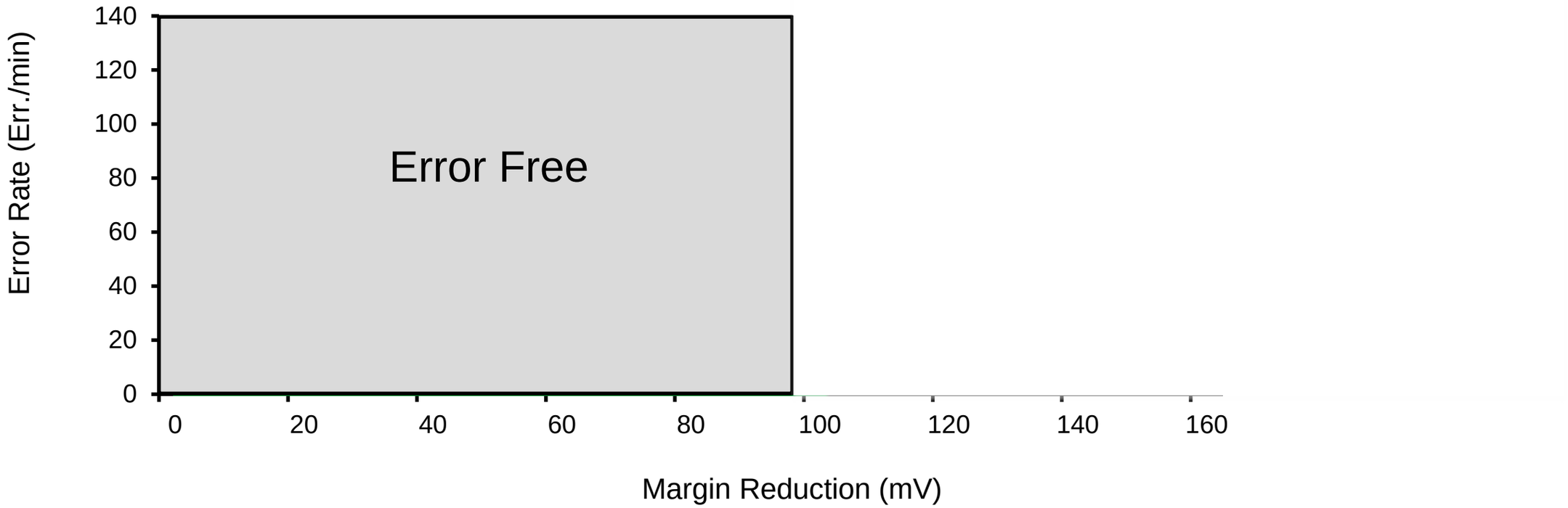
- Margin exploration of 32nm 8-core CMP at two constant frequencies



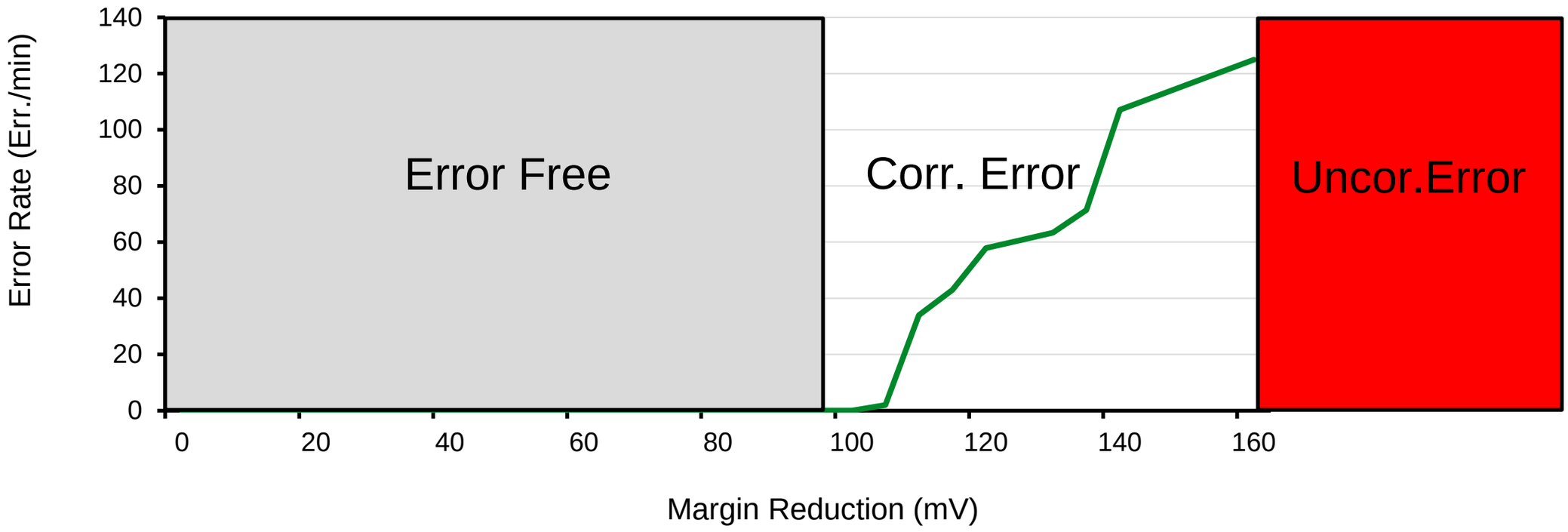
Correctable Errors at Low Voltage



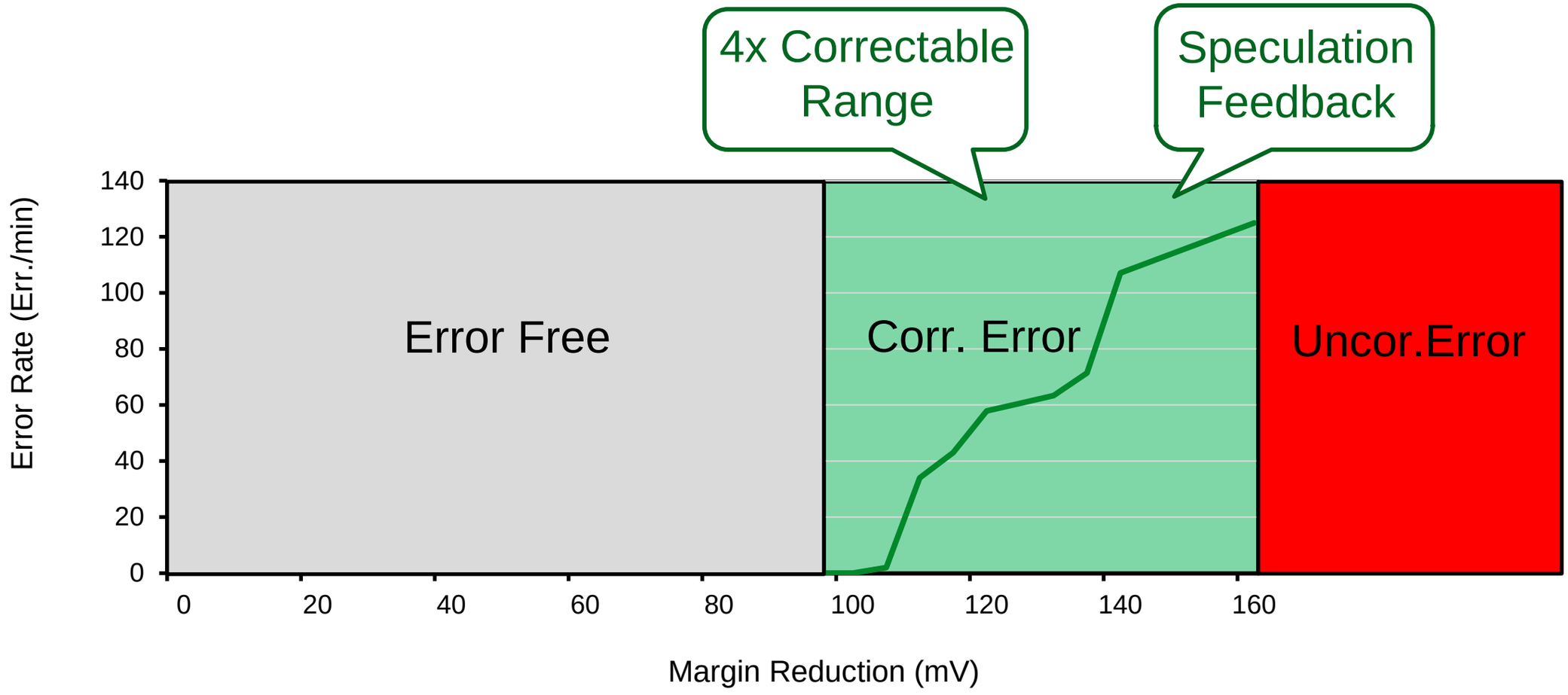
Correctable Errors at Low Voltage



Correctable Errors at Low Voltage

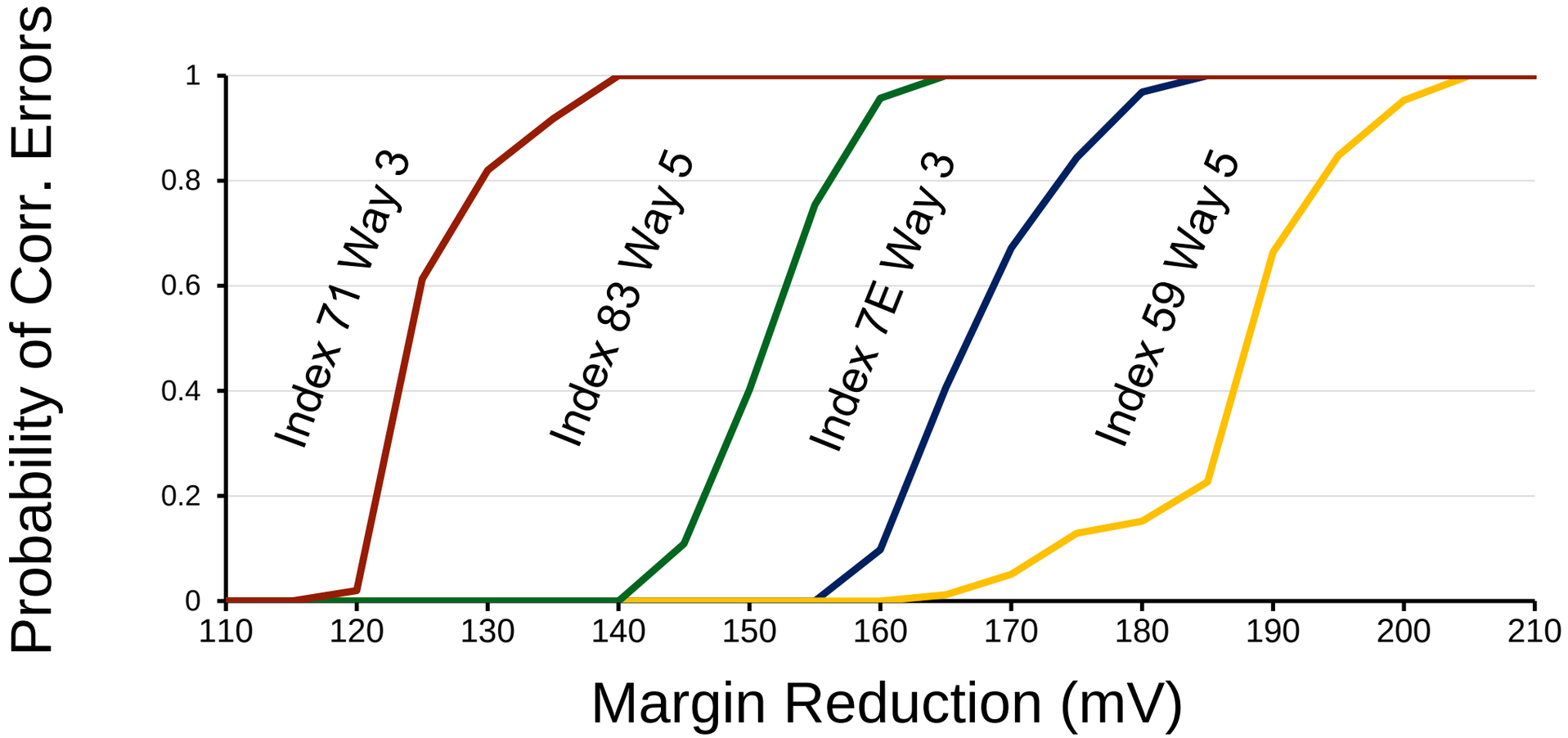


Correctable Errors at Low Voltage



- Large buffer zone for speculation
- Correctable error range is 4x relative to high Vdd

Predictability of Select Cache Lines



Select cache lines consistently react to V_{dd} reduction

Outline

- Motivation
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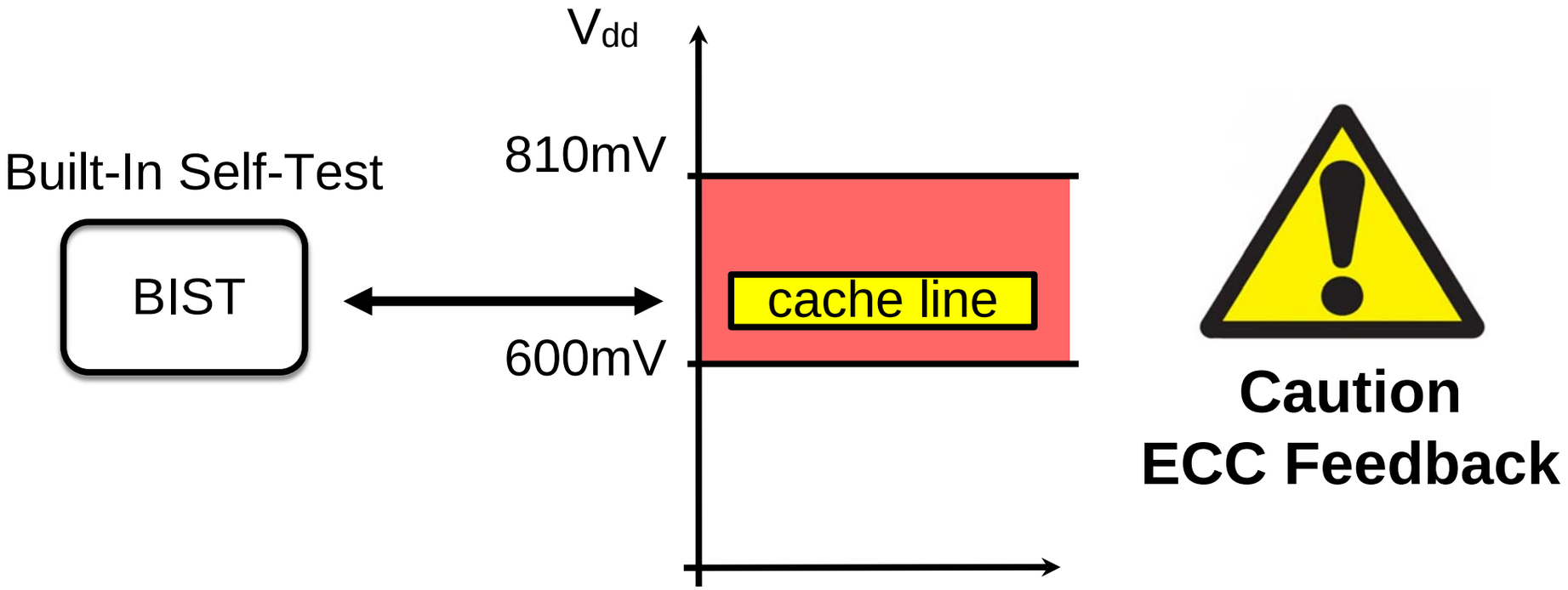
ECC Guided Voltage Speculation

- Main idea:
  - Dynamically lower V_{dd} at constant frequency
  - Treat correctable errors as “early warning system”



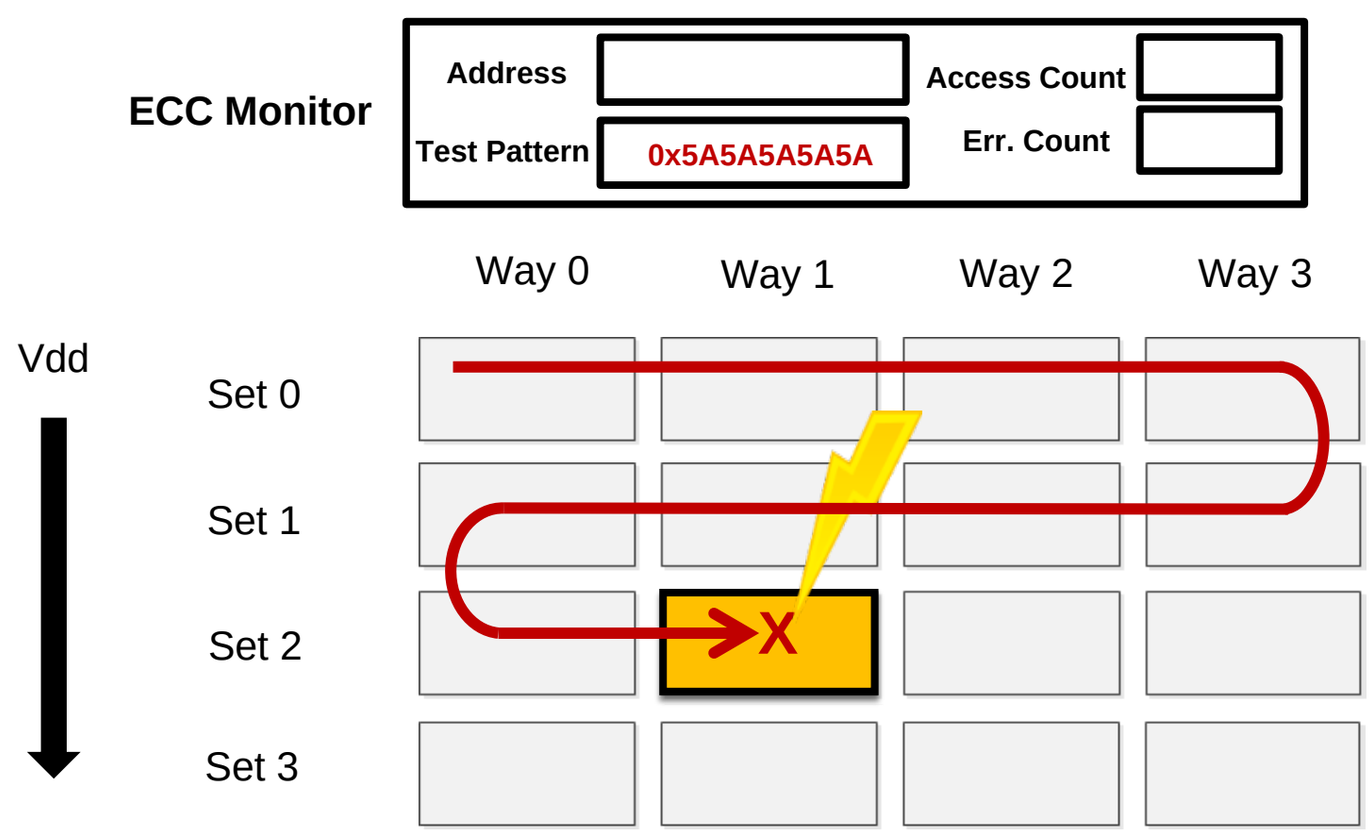
ECC Guided Voltage Speculation

Continuous monitoring of weakest cache line

ECC Guided Voltage Speculation

Continuous monitoring of weakest cache line

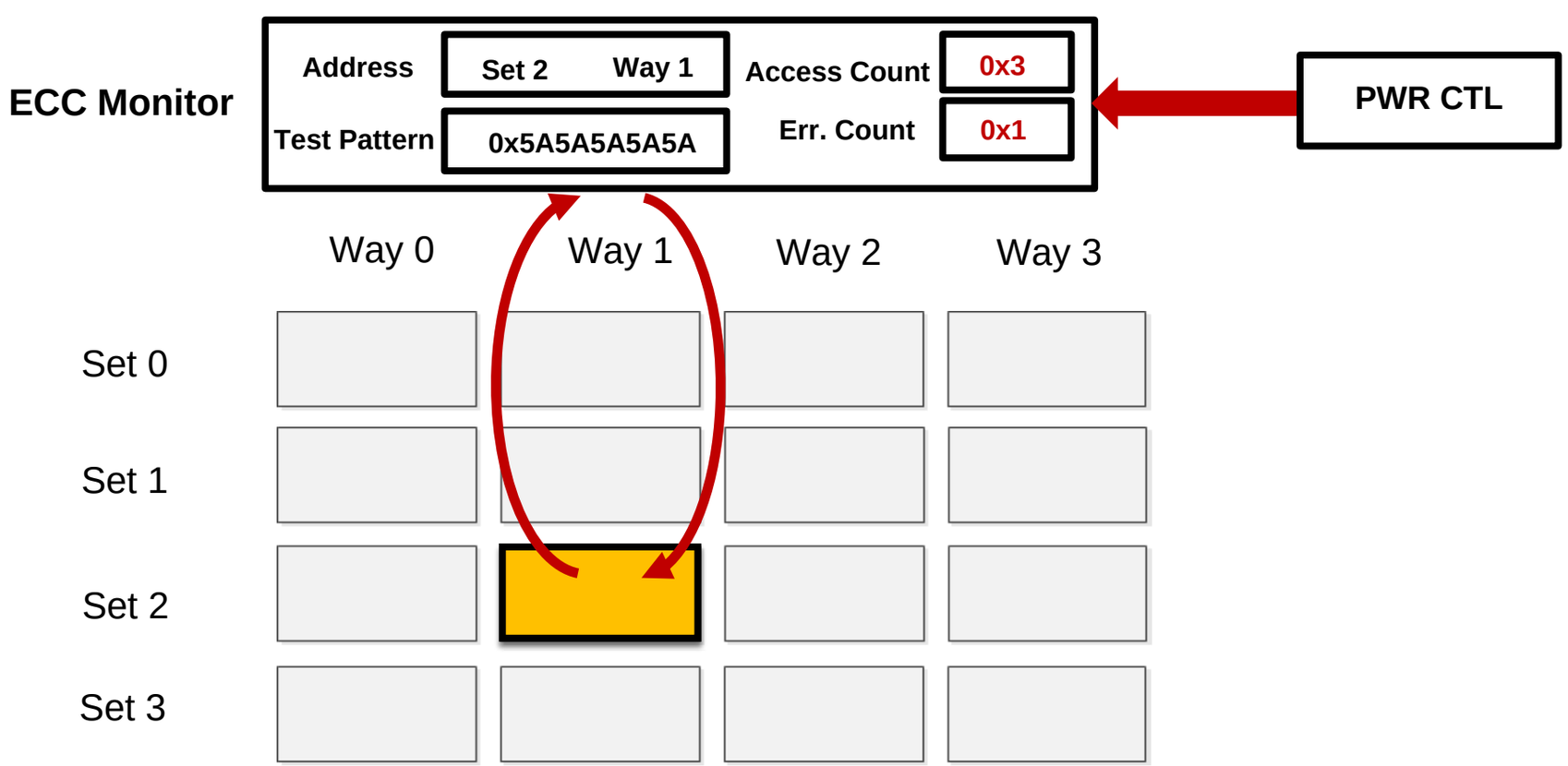
Discovery Phase



ECC Guided Voltage Speculation

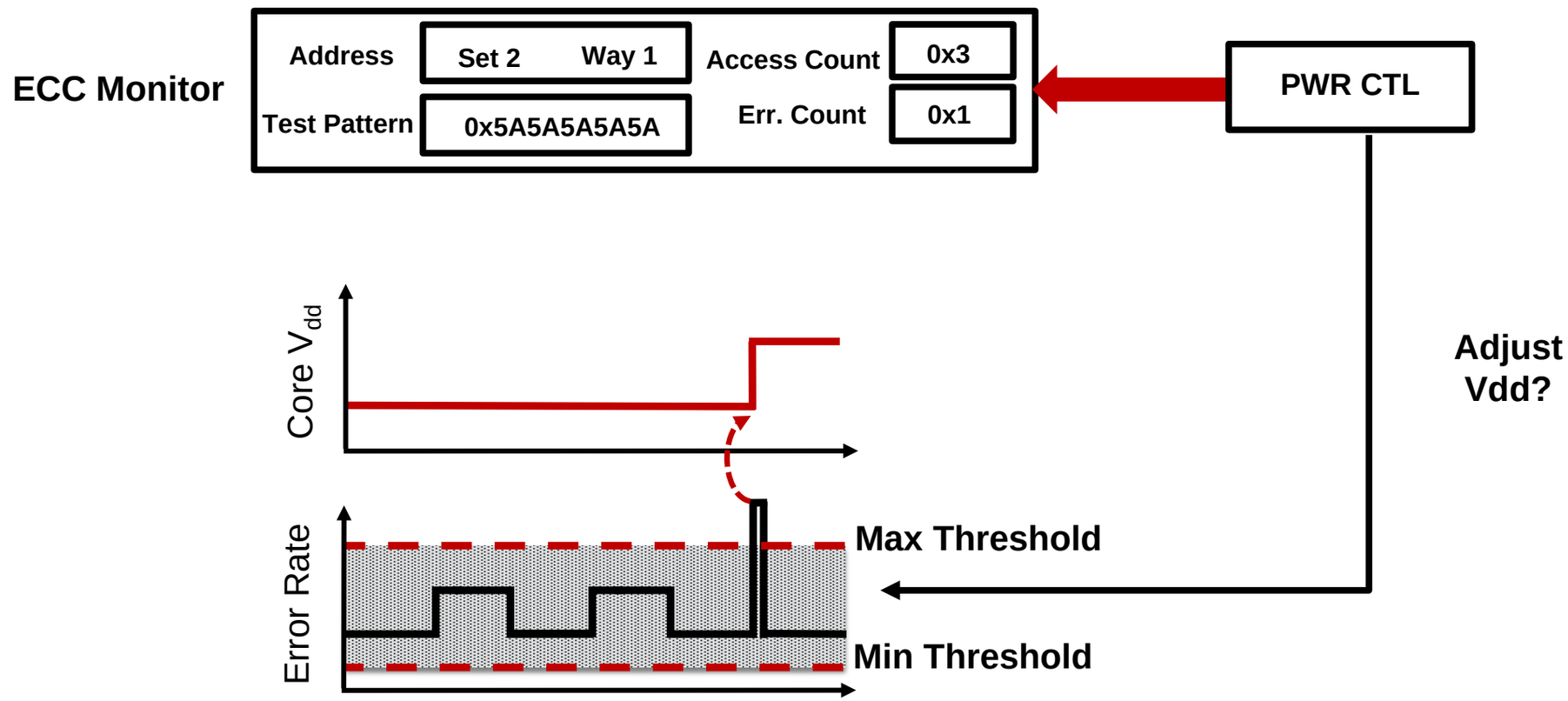
Continuous monitoring of weakest cache line

Runtime Phase



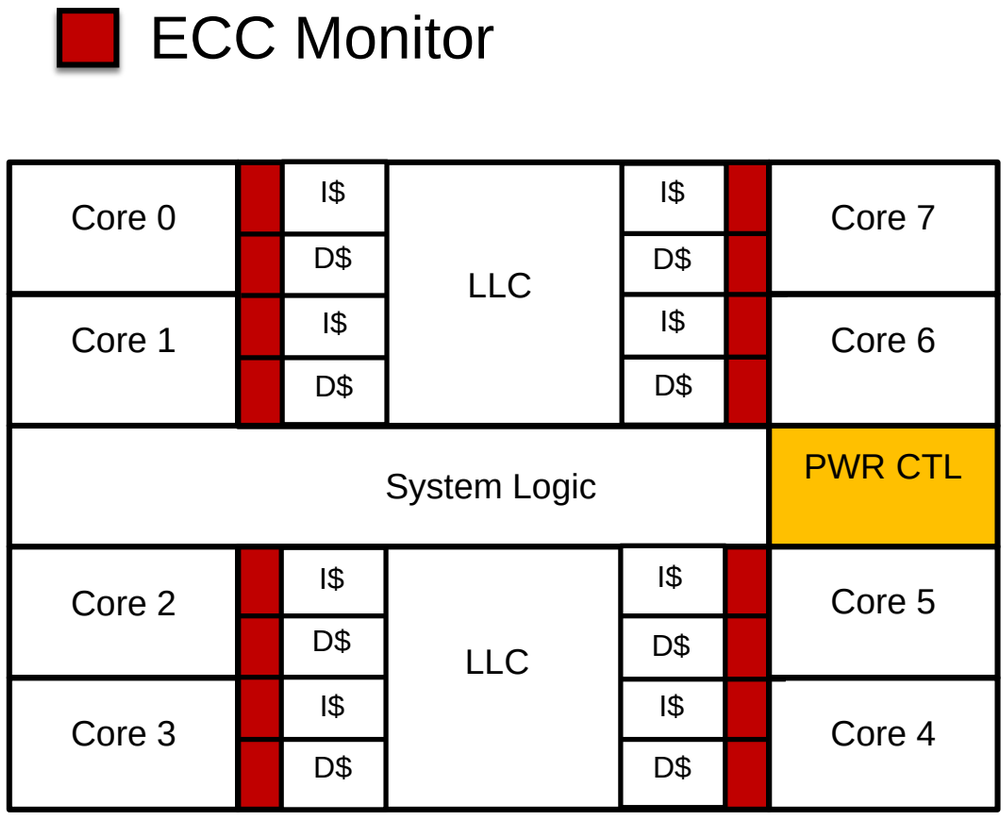
ECC Guided Voltage Speculation

Continuous monitoring of weakest cache line



ECC Monitors and Activation

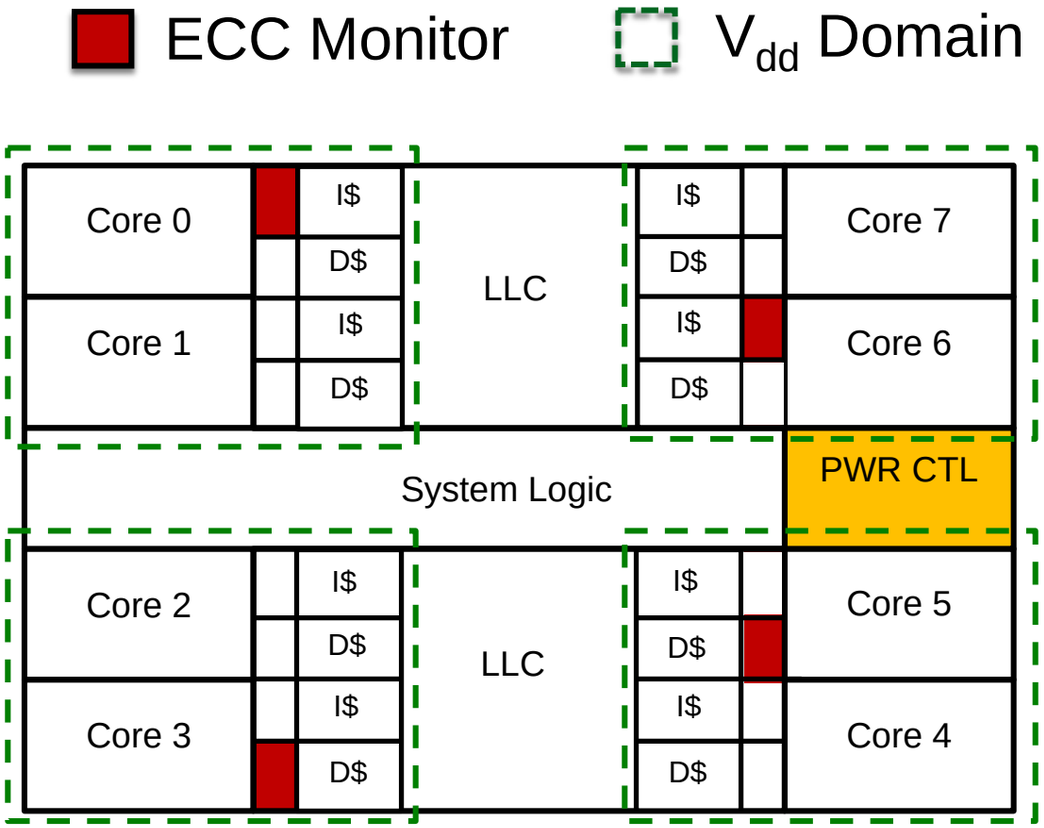
- ECC monitors to probe vulnerable cache lines



8-core CMP with ECC monitors

ECC Monitors and Activation

- ECC monitors to probe vulnerable cache lines
- Activate single monitor across V_{dd} domain



8-core CMP with ECC monitors

Outline

- Motivation
- ECC-based voltage speculation
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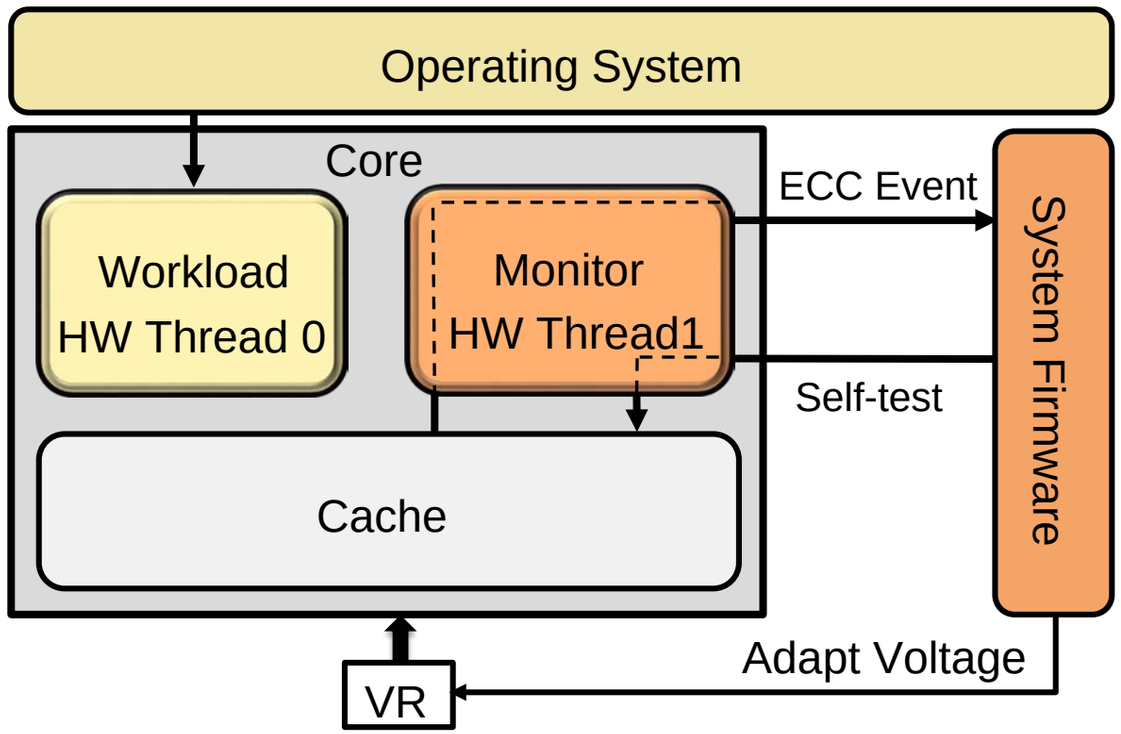
Experimental Framework

- System:
  - BL860c-i4 Integrity Server from HP
  - 2x 9560 Itanium II CPUs

- Simulation (Firmware):
  - HW thread to monitor weak cache line
  - Dedicated “service” core for error logging and power measurements



- Benchmarks:
  - CoreMark, SPEC CPU2000, SPECjbb2005, and stress test application

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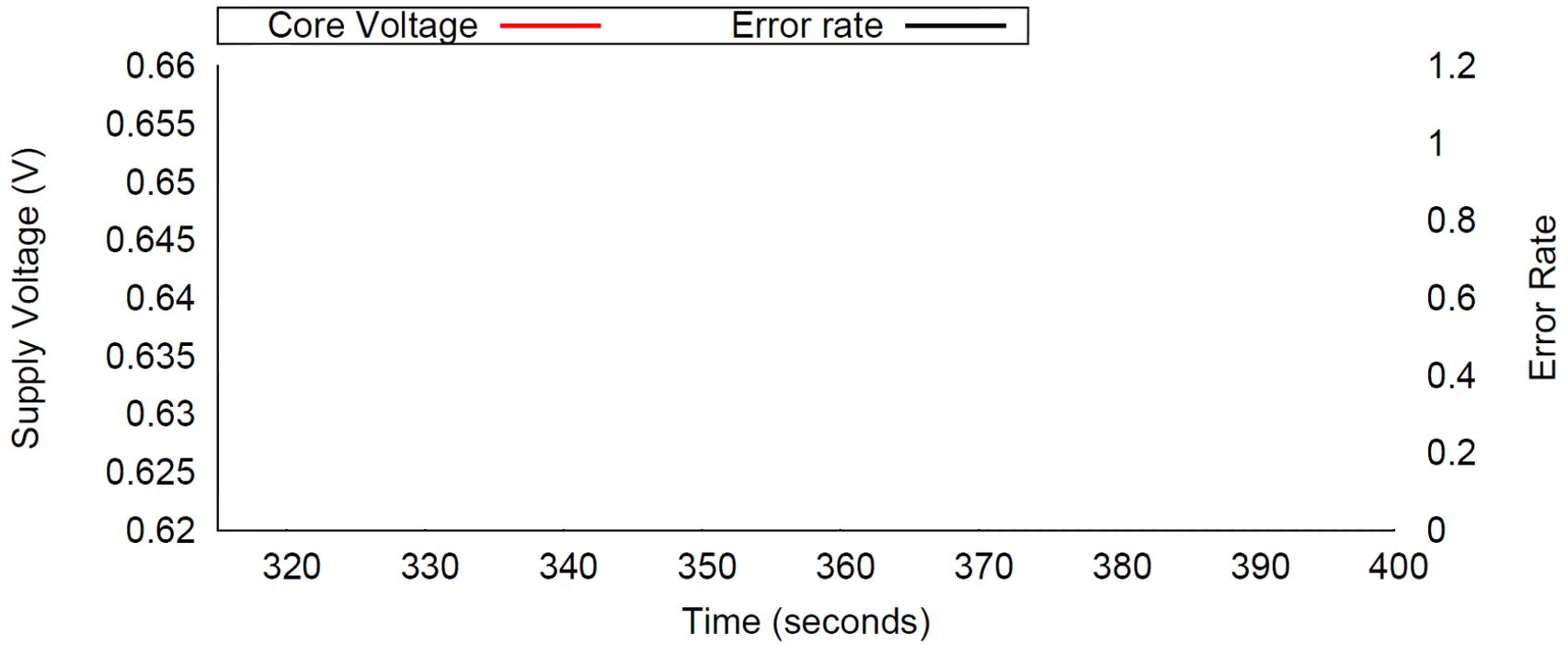
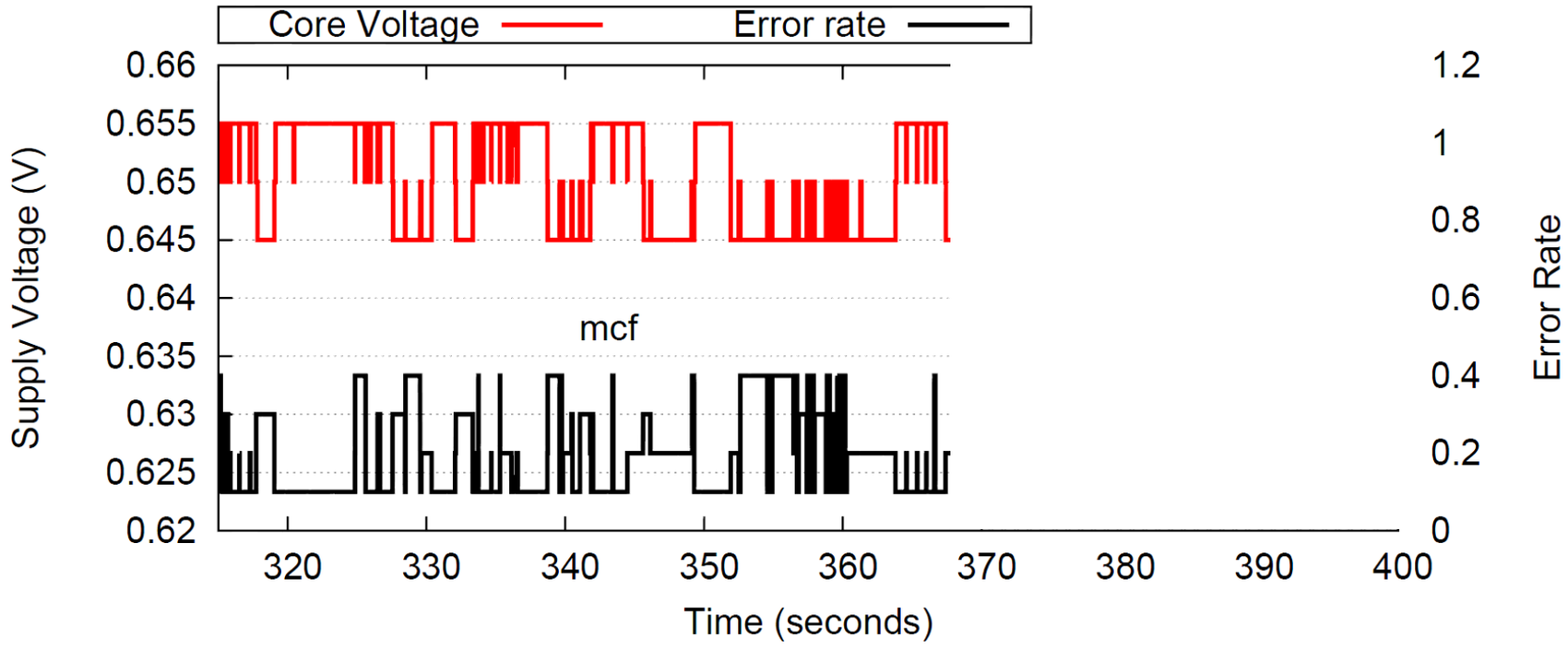
Voltage Speculation in Action



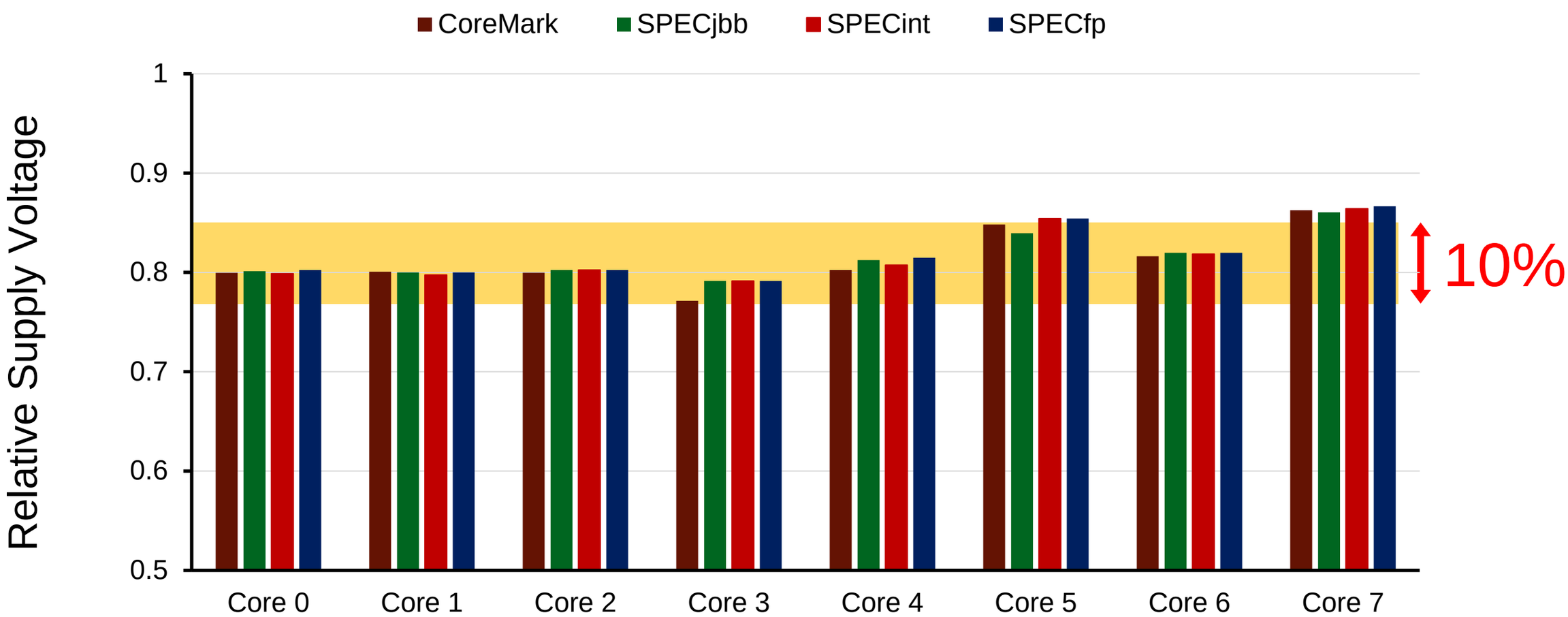
V_{dd} adapts to changing conditions and context switches using error rate as feedback

Voltage Speculation in Action



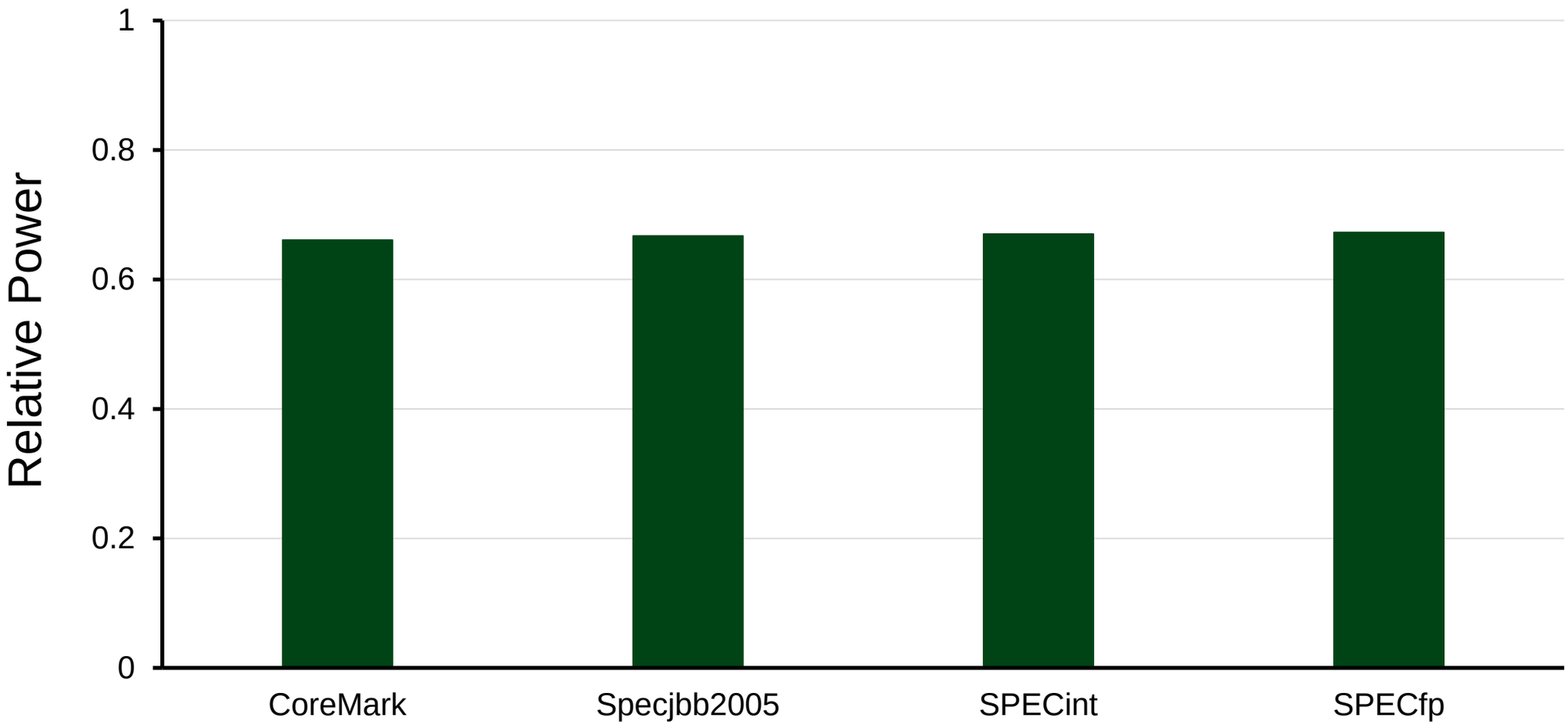
V_{dd} adapts to changing conditions and context switches using error rate as feedback

Supply Voltage Reduction



18% average Vdd reduction

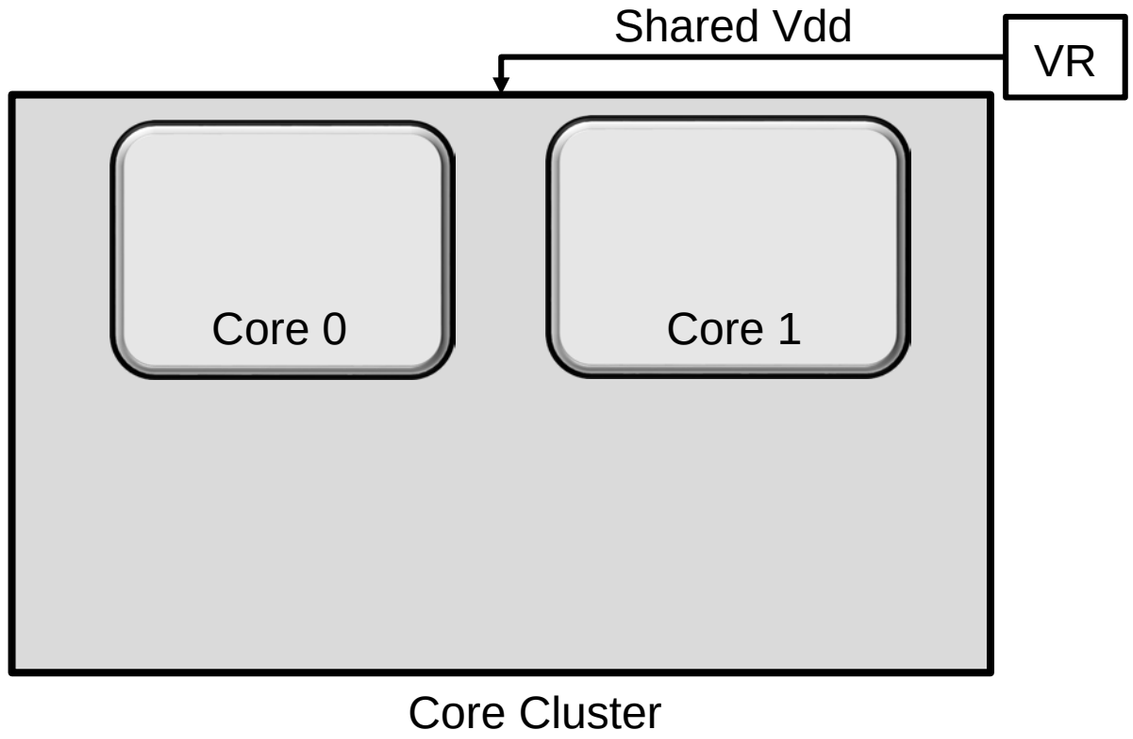
Power Savings



33% power reduction across all cores

Speculation Sensitivity to Workload

- Exploit auxiliary core within core cluster to stress V_{dd}



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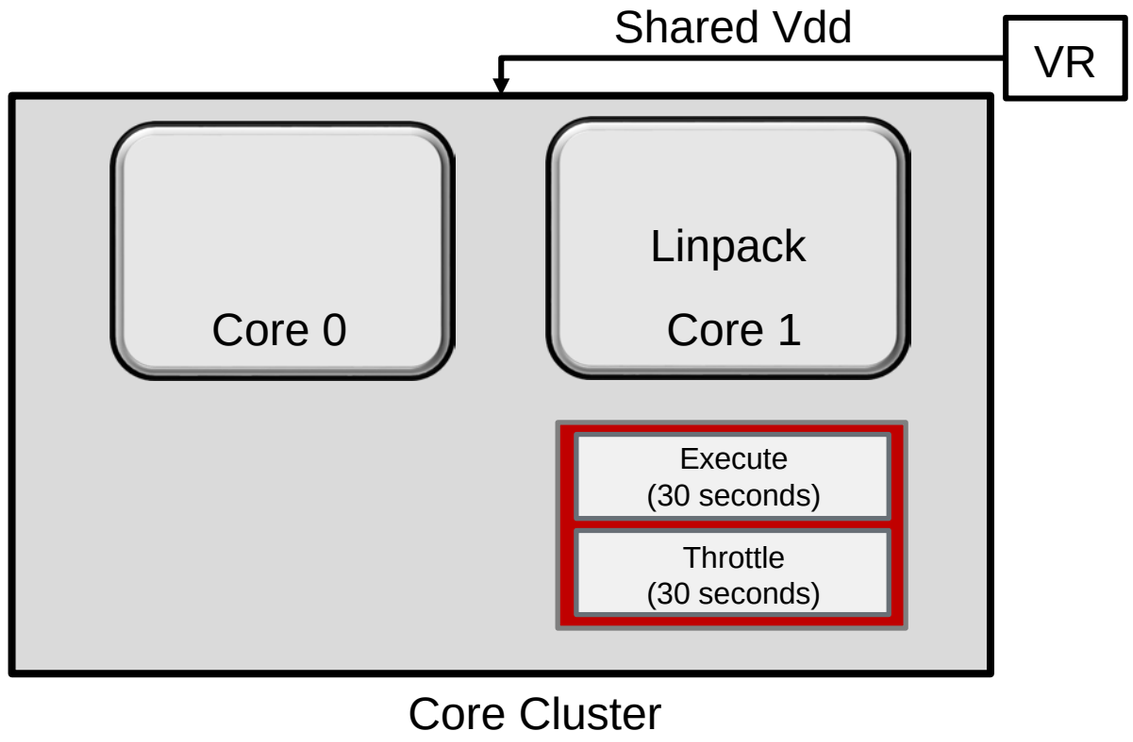

Core Cluster

Speculation Sensitivity to Workload

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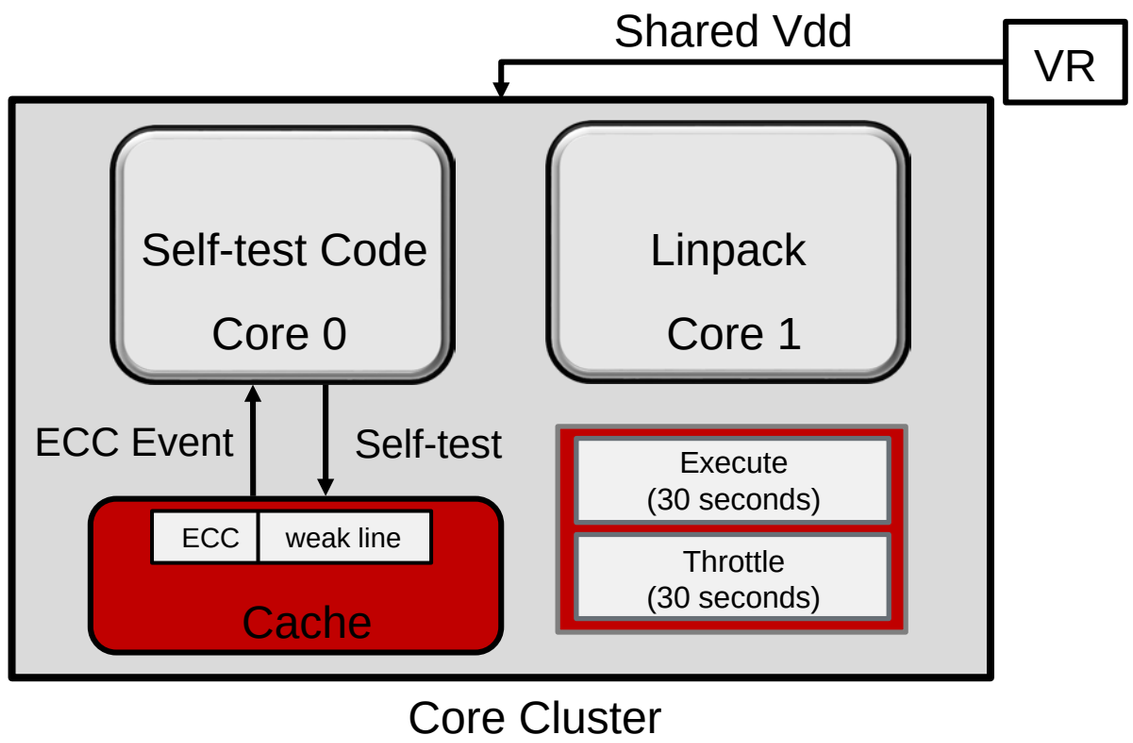

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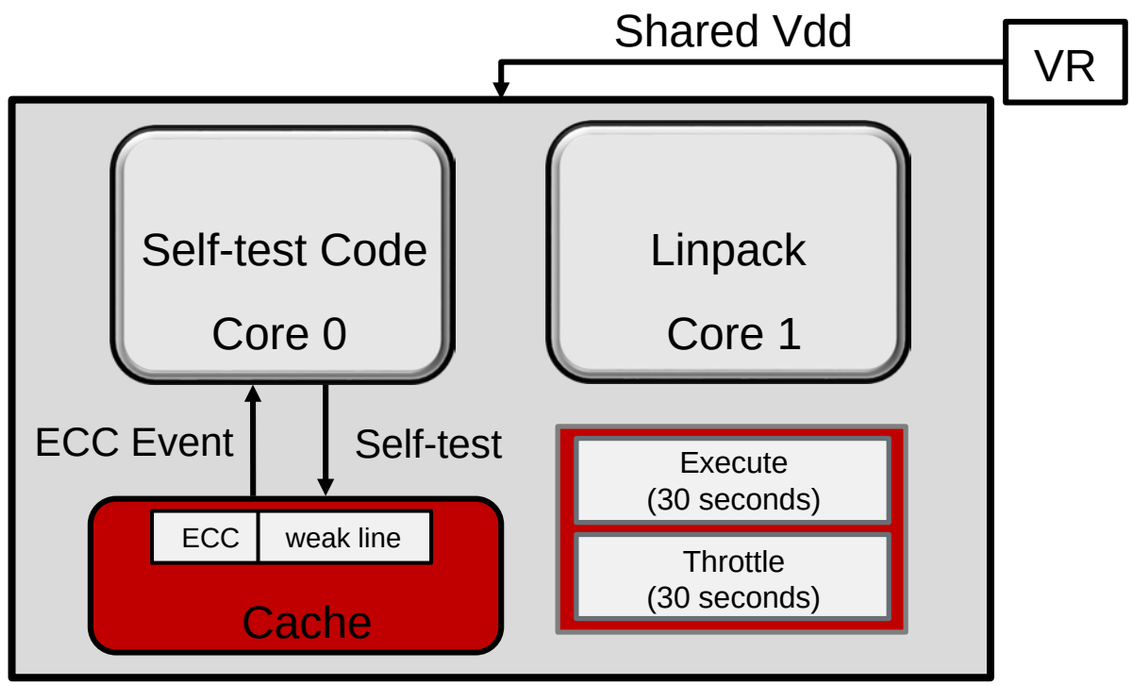
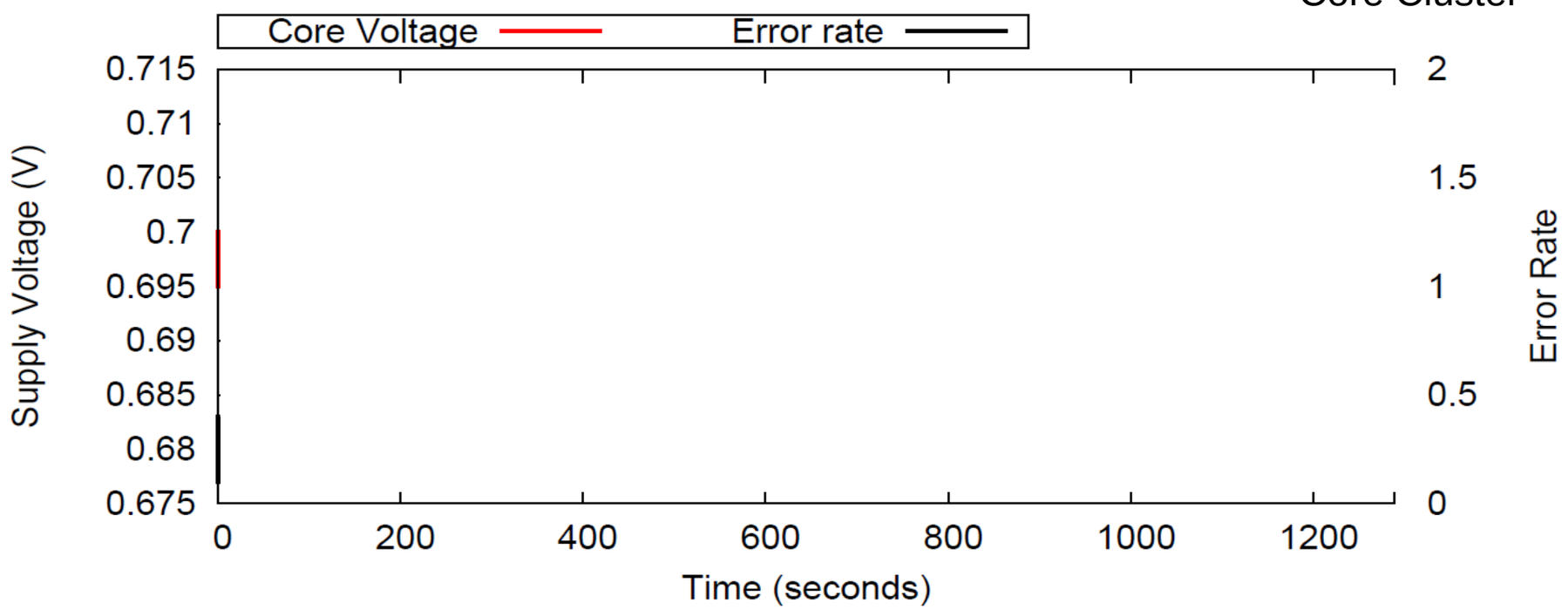
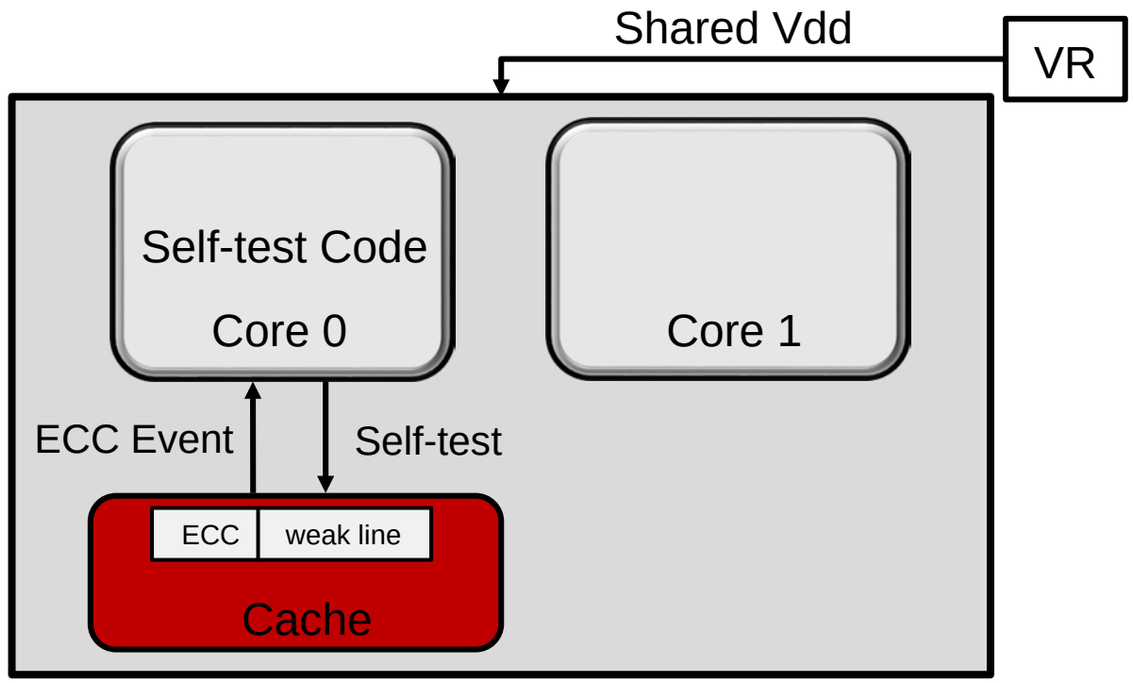




Resiliency to Voltage Noise

- Similarly exploit auxiliary core within core cluster to induce noise



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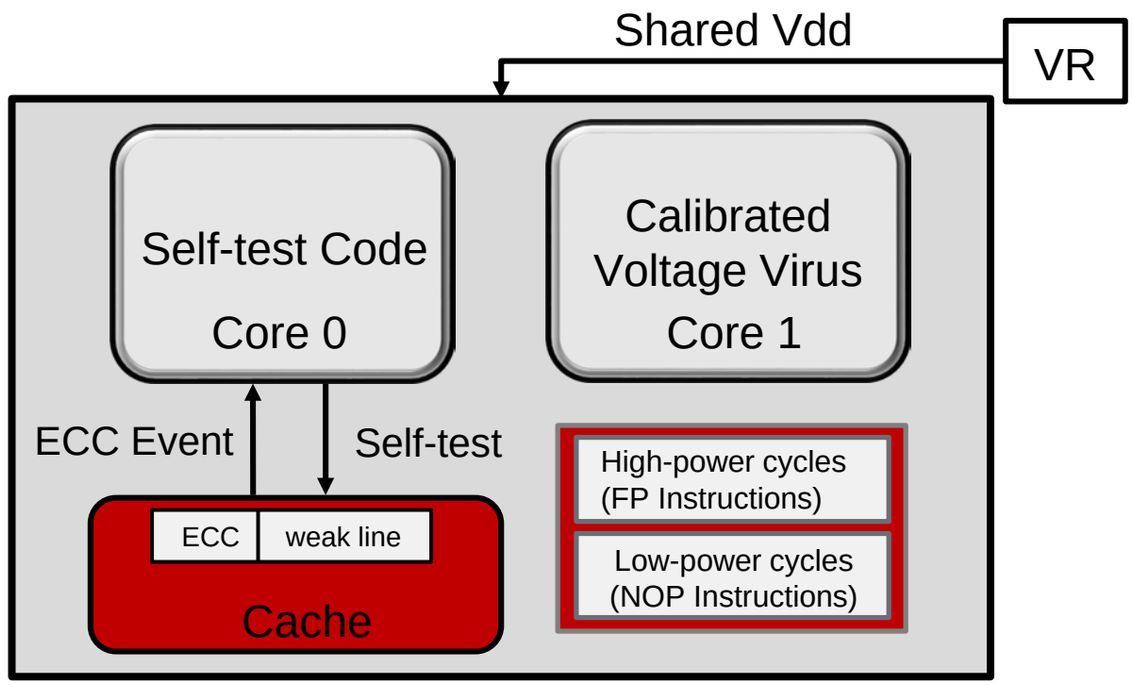

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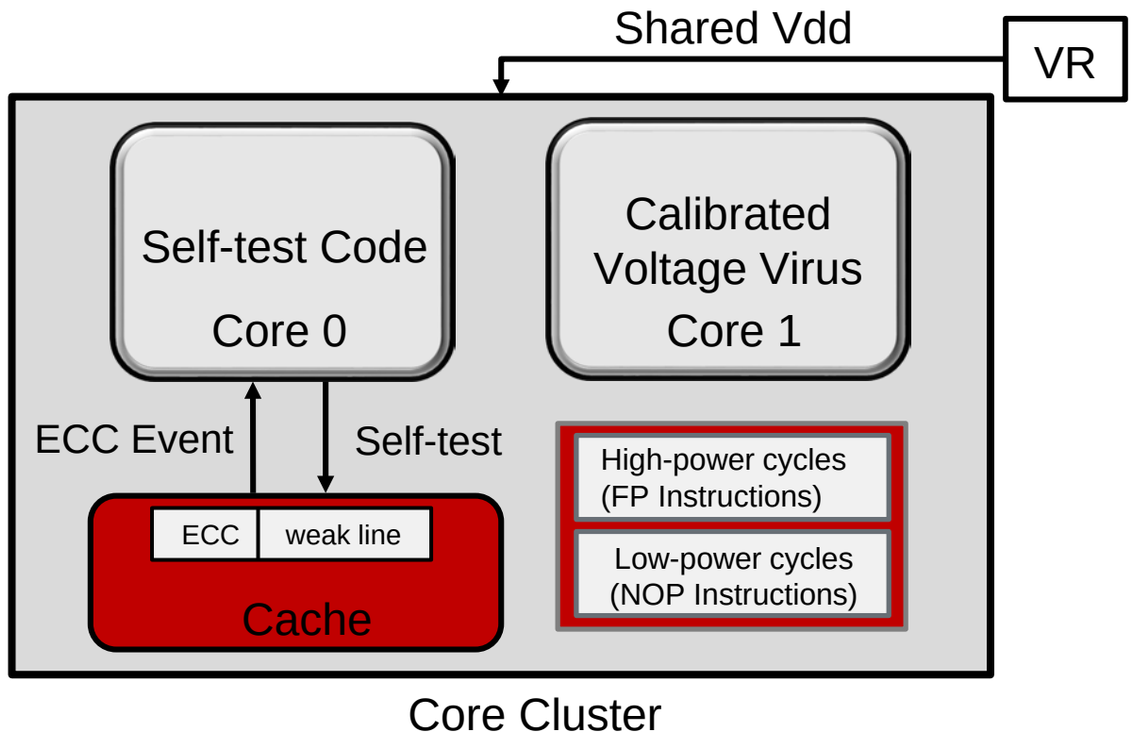
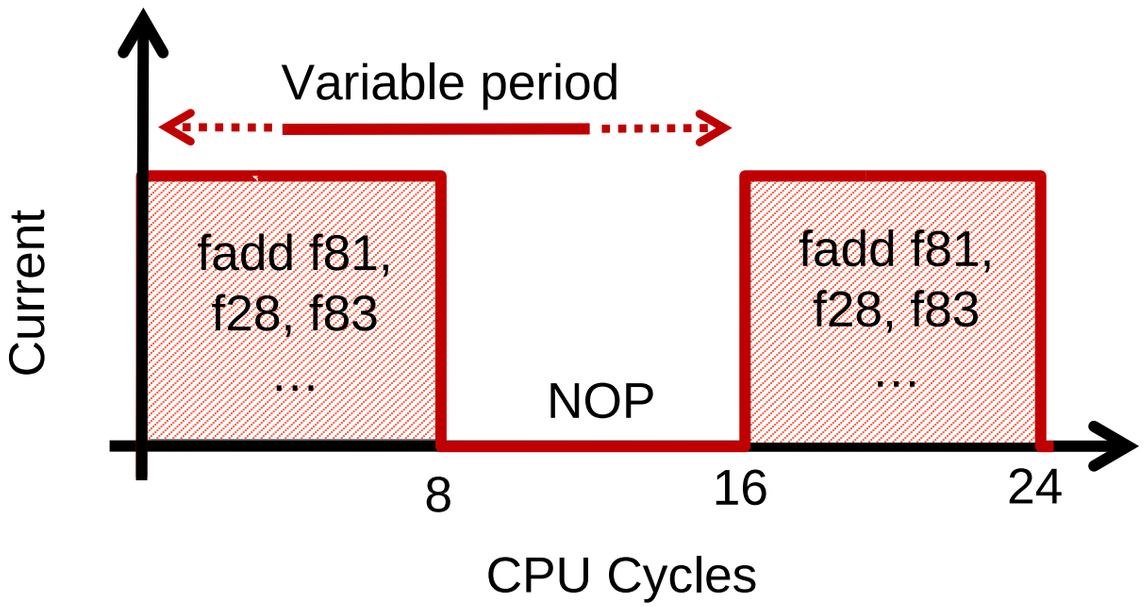


Core Cluster



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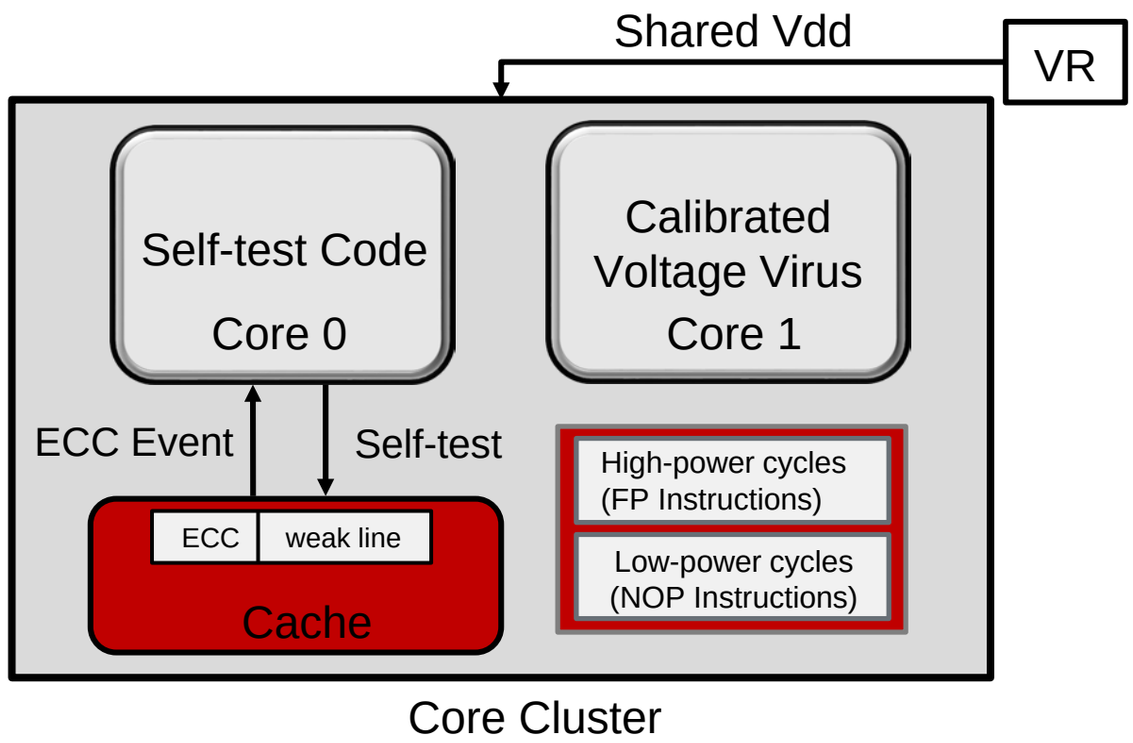

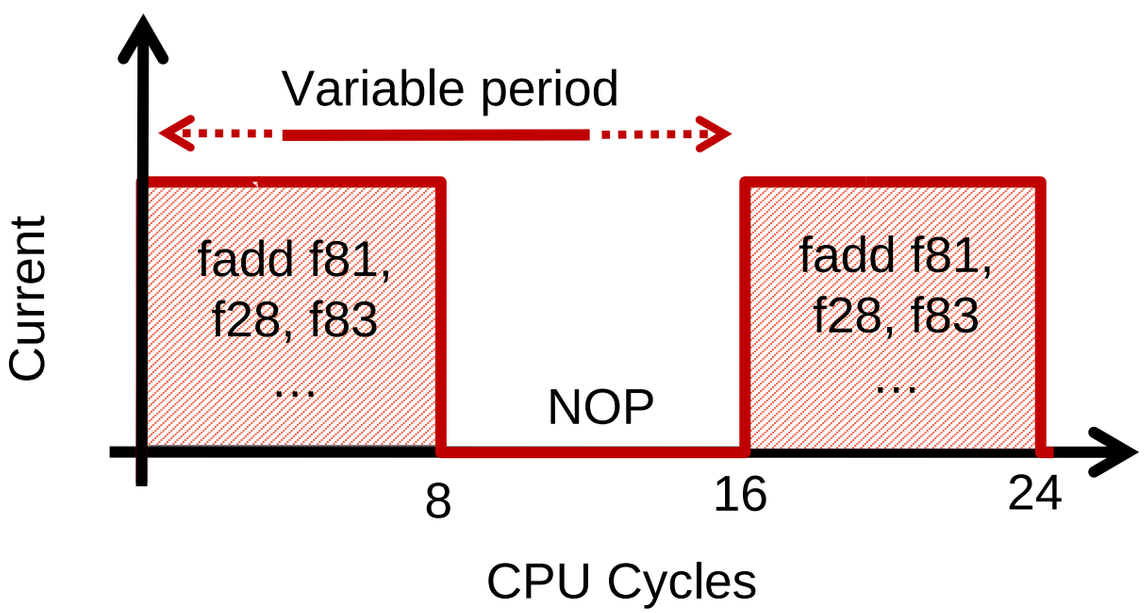

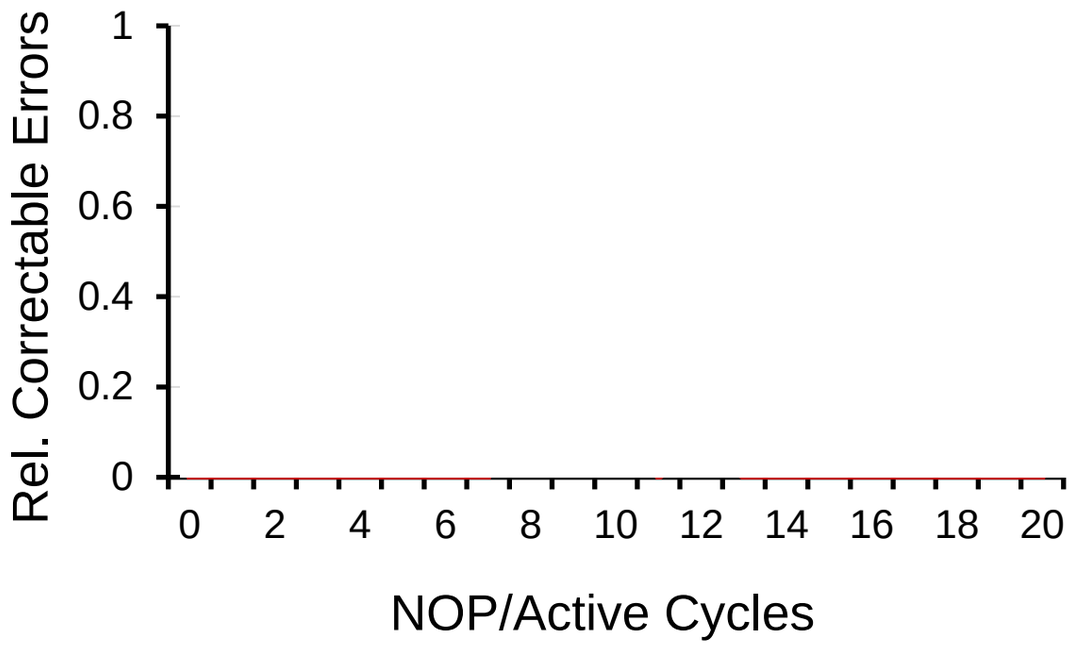

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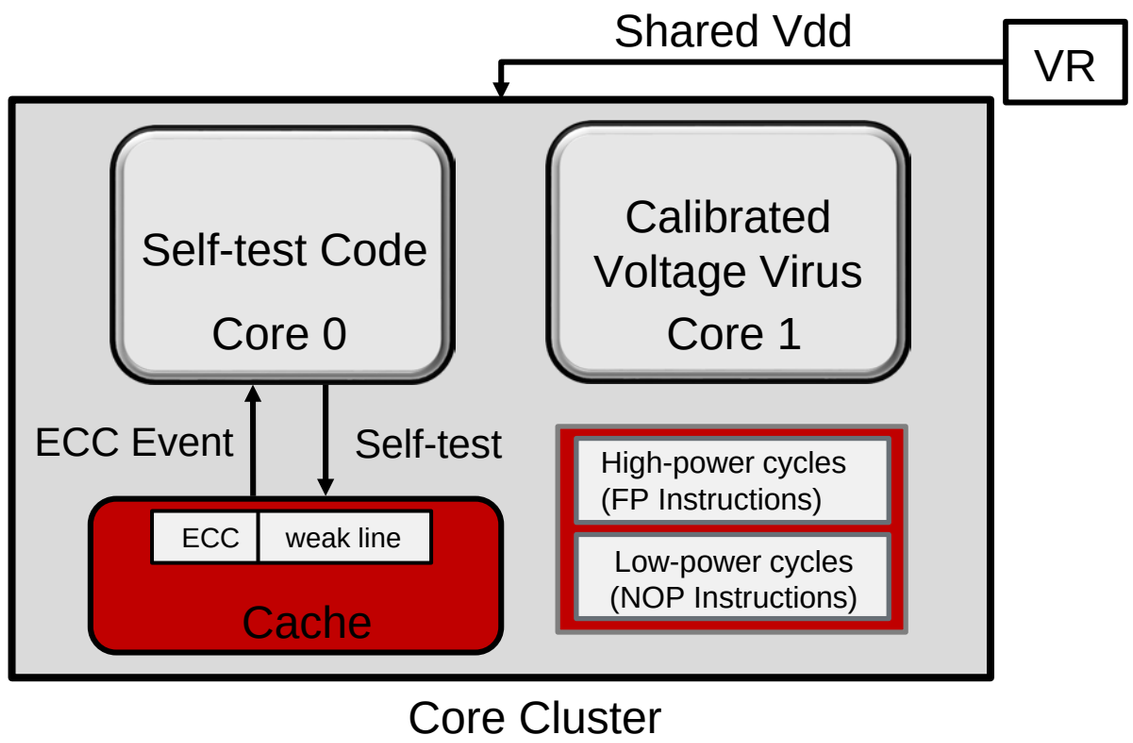
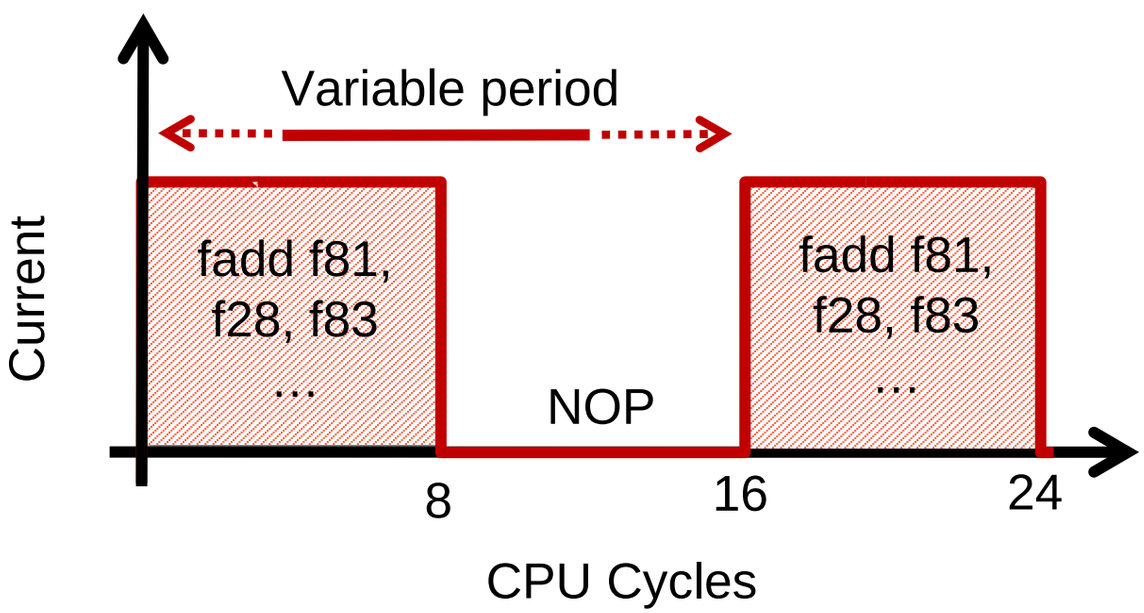
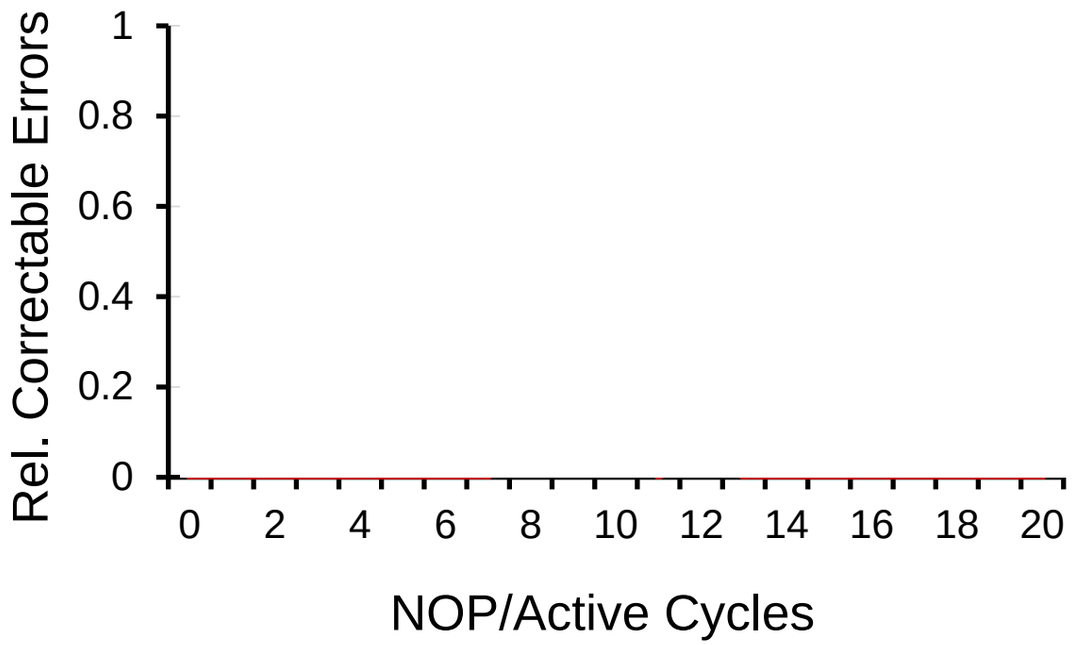
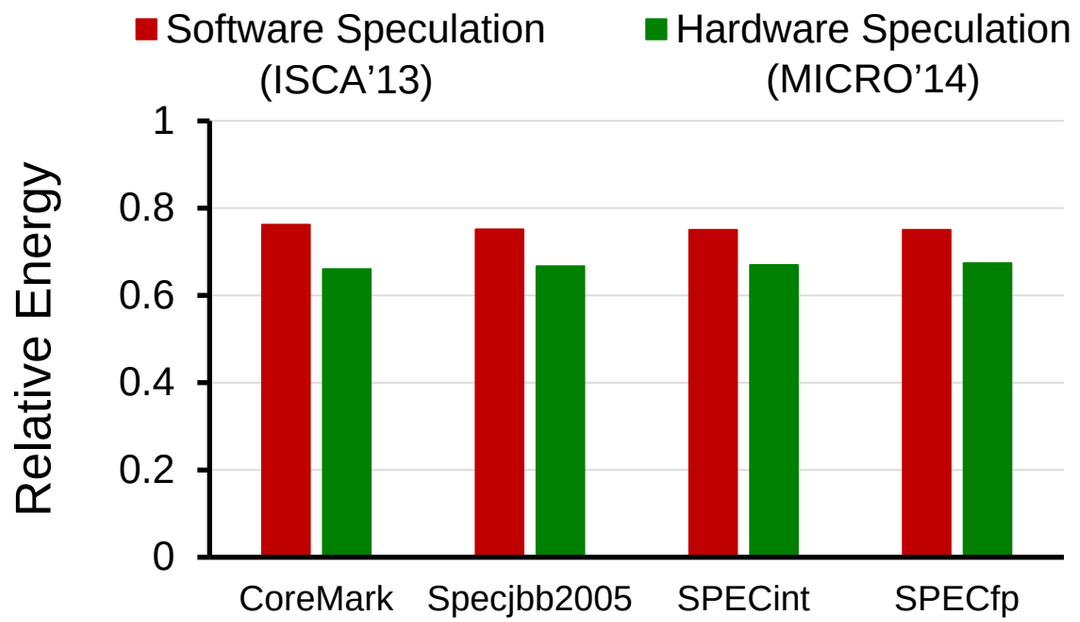




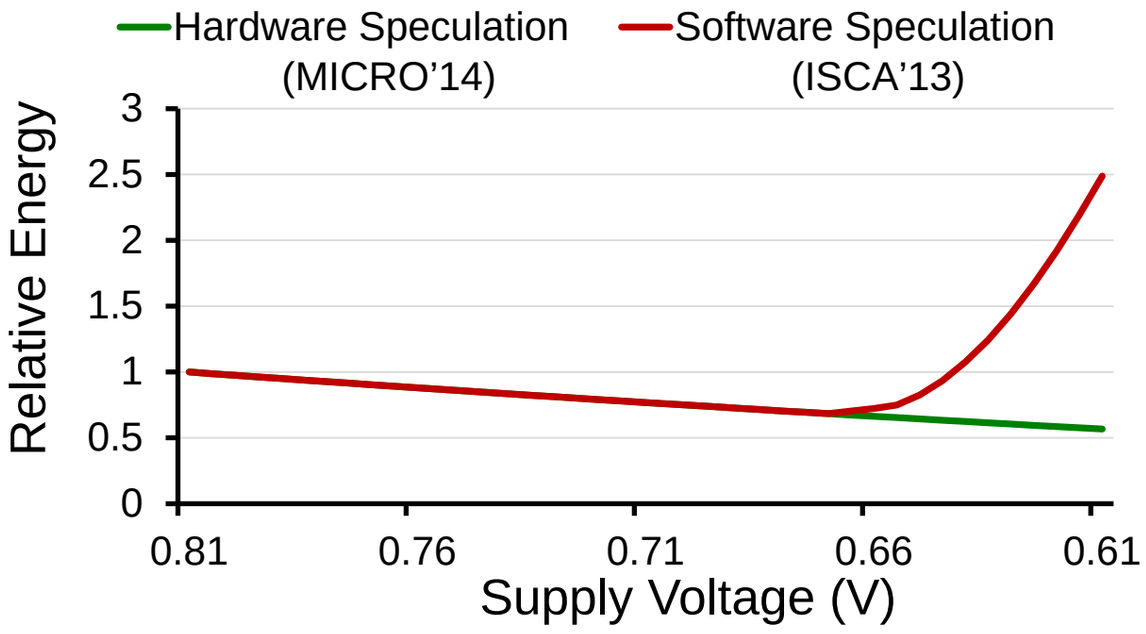


Energy Savings

- 33% in energy savings
  - 11% improvement in energy efficiency over software speculation approach



- Handling errors at low Vdd in software is energy inefficient



Conclusion

- Cache lines can be used for speculation in low voltage
- Demonstrate sensitivity of technique to noise
- Deliver 33% in energy savings
- Evaluate on real system

Thank you!

Questions?

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